DIGITAL STORAGE OSCILLOSCOPE 4035

Instruction Manual

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AMENDMENT SHEET FOR 4035 INSTRUCTION MANUAL

Page 8

1st column.

Add to 'NOTE' -- Allow 20 mins. from SWITCH-ON for the instrument to operate to full specification.

Page 29

Section 4.8 Fast Ram P.C.B. Circuitry.

All 1400 references should read 1800.

Page 30

Section 4.10

1st line Fig 16 to read Fig. 26

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Section 4.19 Power Supplies & C.R.T. Circuits

All 1400 references should read 1300.

PT. NO. 454613

Contents

LIST OF ILLUSTRATIONS

Introduction

The Gould 4035 provides a combination of Digital Storage and Real-time facilities and caters for measurements from DC to 20MHz. The digital method of storage provides many advantages notably the facilities for viewing pretrigger information and displaying waveforms flicker free for an indefinite period. The dual 20MHz analogue to digital convertors maintain the full storage specification for single or dual channel operation for timebase speeds of 50 sec/div to 5μsec/div. Controls are available to lock the data individually for each channel allowing comparisons to be easily made between waveforms.

The analogue output enables the waveforms to be recorded permanently on a chart recorder at a selected output speed. Auto plot will allow any number of captured events to be recorded automatically in a baby sitting mode.

In addition the 4035 has a GPIB Talk only mode, which will send out the contents of the specified store to a digital plotter, in a form accepted by a number of available plotters with a GPIB interface.

The 4035 features two identical input channels with a maximum sensitivity of 2mV/div and a bandwidth from DC to 20MHz. The channels may be displayed separately or together in both Storage or Non Storage modes. The ability to display the sum or difference of the channel inputs and an XY mode operation are available in the Non Storage mode. The timebase ranges are 500ns/div to 0.25s/div in Non Storage and 5μs/div to 50s/div in Storage mode. A x 10 facility expands the upper sweep speed to 50ns/div in Non storage and gives expansion to observe the full detail of the Ik word stored traces.

A pair of cursors are available on either trace, for convenience in making measurements on the traces. A 16 character display on the screen displays the time and voltage difference between the two cursors.

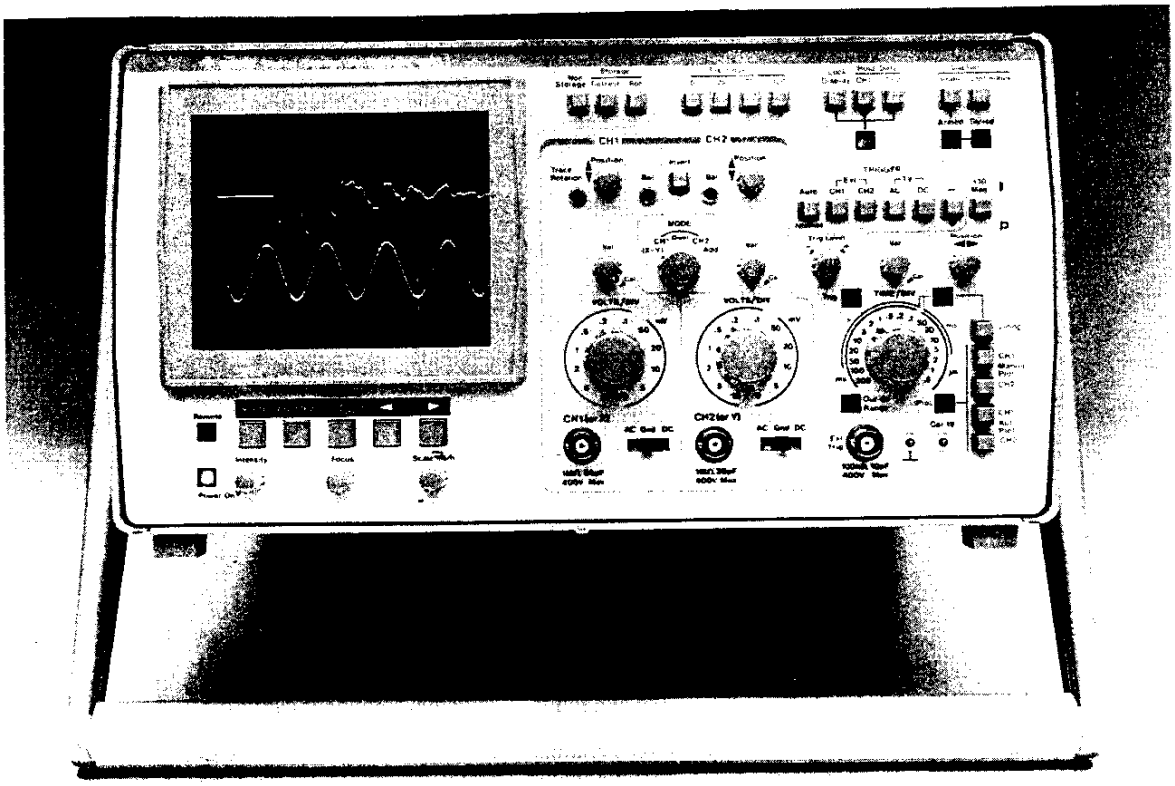
A GPIB interface is fitted, so that a GPIB controller (eg a microcomputer) can obtain stored trace information from the oscilloscope and if required, send a trace to the screen. It also permits remote control of the oscilloscopes digital controls.

Variable controls are available for input sensitivities and Non storage timebase speeds.

The comprehensive trigger facilities have an 'auto' function to assist the operator by ensuring a trace is present in the absence of trigger. AC & DC coupling and either channel or external source selection with a line supply at the rear panel ensures the appropriate trigger is available for all applications. An active TV sync separator is provided for viewing or storing video waveforms.

Additional facilities are provided such as 1kHz calibrator signal, a DC coupled Z modulation input and a trace rotational control.

The instrument is portable and the use of a large custom integrated circuit has reduced the number of components with the benefit of reliability and ease of maintenance.



Specification

Section 2

DISPLAY

CRT 8 x 10cm rectangular.

EHT 2kV
Internal illuminated Graticule with 8 x 10 cm divisions and 2mm sub-divisions.
Continually variable illumination.
Trace Rotation by front panel preset.
Alpha-numeric 16 character display for messages and measurements 8 x 7 dot matrix.

VERTICAL DEFLECTION

Two identical input channels CH1 and CH2.

Bandwidth DC–20MHz (–3dB) DC coupled.
(2Hz–20MHz) AC coupled in the non-storage.

Sensitivity 2mV/div to 10V/div, 12 ranges in 1–2–5 sequence.

Accuracy ±3%

Variable Sensitivity > 2.5.1 range allows continuous adjustment of sensitivity 2mV/div to 25V/div.

Input Impedance 1MΩ/25pF.

Input Coupling DC–GND–AC

Input Protection 400V DC, or pk AC.

HORIZONTAL DEFLECTION

Non-storage

Sweep Rates 0.5μs/div to 0.2s/div 18 ranges in 1–2–5 sequence.

Accuracy ±3%

Variable Sweep > 2.5.1 allows continuous coverage from 0.05μs/div to 0.5s/div.

Expansion X10 push button gives up to 50ns/div. Accuracy ±3% (50ns ± 5%).

Storage

Sweep Rates 5μs/div to 50s/div. 22 ranges in 1–2–5 sequence incorporating X1000.

Accuracy ±3%.

Expansion X10 push button gives up to 500ns/div. Accuracy ±3%.

TRIGGER

Variable level control with Auto/Normal facility. In 'Auto', the timebase runs when insufficient signal (20Hz to 20MHz) is present, or when the selected level is outside the range of the input signal.

Source Internal CH1 or CH2, or External.

Slope +ve or –ve.

Coupling DC, AC or TV.

Note: TV Active sync separator with line/frame selected by timebase with:-

Field rate from 0.2sec/div to 100μs/div.
Line rate from 50μs/div to 0.5μs/div.

Internal Sensitivity
DC coupled 0.3div to 2MHz.
1.5div to 20MHz.
AC coupled 0.3div, 10Hz to 2MHz.
1.5div, 4Hz to 20MHz.

External Sensitivity
DC coupled 150mV to 2MHz
600mV to 20MHz
AC coupled 150mV, 10Hz to 2MHz
600mV, 4Hz to 20MHz

External Input Impedance 100kΩ/10pF approximately

External Input Protection 250V RMS, 400V pk.

Line Trigger Source Rear panel output via bnc nominally 8V pp.

DISPLAY MODES

Single Trace CH1 or CH2.

Dual Trace Non-storage, Chopped or Alternate Modes, automatically selected by the timebase switch. Between 0.5μs/div and 0.2ms/div the Alternate Mode is selected whilst on ranges slower than 0.2ms/div Chop Mode is selected. The Chop frequency is 500kHz. (In Storage Mode the capture is simultaneous).

Add CH1 and CH2 added to give the algebraic sum of the two channels inputs (Non-Storage Mode only).

Invert CH2 may be inverted. When used in conjunction with Add Mode, it gives the algebraic difference of the two channels.

X–Y CH1 gives X deflection and CH2 input gives Y deflection. (Non-Storage Mode only).

DIGITAL FACILITIES

Store Size 1024 x 8 bits/channel.

Vertical Resolution 1 in 256.

Horizontal Resolution 1 in 1024.

Expansion X10

Maximum Data Conversion Rate 20MHz/channel.

Dot Joining Linear Interpolation between samples.

STORAGE MODES

Roll Stored data and display updated continually. (Timebase ranges 50s/div to 5μs/div).

Refreshed Stored data and display updated by triggered sweep. (Timebase ranges 50s/div to 5μs/div).

Continuous Capture Updates display each time a trigger occurs.

Single Capture Freezes at end of triggered sweep.

Lock Display Freezes store immediately.

Lock CH1 Holds CH1 store immediately.

Lock CH2 Holds CH2 store immediately.

Pre-Trigger Storage Switchable for 0%, 25%, 75% and 100% of full store pretrigger, available in Roll Mode only.

CURSOR MEASUREMENTS

Controls On/Off control of Alpha-numerics and cursors. Selection of channel for measurement CH1/CH2. Set datum to current cursor position. ◀ ▶ Dual speed cursor position (left/right) to enable time and voltage difference measurement.

Accuracy Time ±0.1% of full scale deflection

Voltage 3% of reading ±0.5% of full scale ±1 digit.

INPUT/OUTPUT FACILITIES

External Clock Input/output CMOS compatible, 5V.

Master Arm Input/output CMOS compatible, 5V.

Acquisition Gate Output CMOS compatible, 5V.

Slave Enable Input CMOS compatible, 5V.

The signal inputs/outputs enable instruments to be used as Master/Slave for multi-channel single shot capture.

External Arm Input CMOS compatible, 5V.

External Arm Enable Input CMOS compatible, 5V. Enables the 4035 to be "Armed" from an external source. Connections via 15-way D type connector on the rear panel.

PLOT OUTPUT

Digital Plot In digital plot mode the IEEE–488 Interface is used in Talk Only Mode HPGL format, to output the data and range to a digital plotter.

Scale Automatically printed.

Graticule Available for plotting at the completion of plot cycle by selection of 'set datum'.

Colours Colour pens automatically selected for CH1, CH2 and graticule when available on plotter.

ANALOGUE PLOT

Analogue Output of the stored display suitable for X–Y or T–Y Chart Recorders.

Y Output Channel 1 and Channel 2 simultaneously via 4mm sockets.

Amplitude 100mV/div. (±10%).

X Output X ramp via 4mm socket.

Amplitude 100mV/div. (±10%).

Output Sweep Rate selected by a switch on the rear panel.

Ranges 0.1sec/div – 20sec/div in 8 ranges. (1–2–5 sequence)

Output Impedances 100Ω

Pen Lift Isolated single pole contact closes from start command to end of:-

Rating: 100VDC, 250mA, 10WDC.
Isolation: 100Vmax.
Connection via 15-way D type connector on the rear panel.

Plot Mode Manual plot of Channel 1 or Channel 2 selected via the front panel switch.

Auto Plot of Channel 1 and Channel 2 or both sequentially selected via the front panel switches.

GPIB INTERFACE

The IEEE–488 Interface enables the 4035 to transmit and receive data and control settings.

SH1	Source Handshake
AH1	Acceptor Handshake
T5	Basic Talker serial poll
L4	Basic Listener
SR1	Service Request
RL1	Remote/Local
PP0	Parallel Poll, no capability
DC1	Device Clear
DT0	Device Trigger, no capability

Full capability except where stated.

Read and Write Functions
Stored Data format Binary, Decimal, Hexadecimal, Octal and string length.
Roll/Refresh Modes
CH1, CH2 and Dual.
Plot and Plot Rate.
Lock display.
Pretrigger range
Timebase range
Arm and Release.

Read Only
Non-storage Mode.
CH1, CH2 and Dual.
Attenuator Timebase setting current and stored.
CH1 stored and CH2 Hold.

Write Only
Text

Talk Only Mode
Data output only format set by internal switch fixed block size of 80 characters for printer output.

Specification

Section 2

SUPPLY
100V, 120V, 220V and 240V ±10% 45 to 400Hz, 100VA approx.

SAFETY
Designed for IEC348 Cat.1 Standards.

OPERATING TEMPERATURE RANGE
50°C (+ 15 to + 35°C for full accuracy).

DIMENSIONS
Size: 335mm width x 178mm height x 479mm depth,
13.2" x 7" x 18.9"
without handles
380mm x 168mm x 555mm
14.95" x 7.3" x 21.85"
with handles

Weight: 11.8kg (26lb)

ACCESSORIES SUPPLIED
Handbook: PN453485
Supply Lead: PN402001

OPTIONAL ACCESSORIES
Probe Kit PB12
A passive probe kit with switched X1 and X10 attenuators.
X10 attenuation input impedance is 10MΩ/11.5pF.

Probe Kit PB13
An X10 passive probe with 1.5m of cable.
Input impedance 10MΩ/11.5pF.

Probe Kit PB17
An X100 passive probe with 1.5m of cable.
Input impedance: 100MΩ/4.5pF.
Working Voltage: 1.2kV inc pk AC.

Viewing Hood: PN452985

Front Panel Cover: PN452986

Rack Mount Kit: PN452987

Rack Mount Tray with slides: PN452988

Trolley, Type TR7 General Purpose

Protective Carrying Case:
PN452989 – A strong case enclosing the oscilloscope with three thicknesses of padded material covering the front panel.

SIGNAL CAPTURE FUNCTIONS
Signal Averaging Steps selectable from 1, 4, 8 or 16.

TV Line Locks onto selected TV line numbers. (Actual lines dependent on transmission system).

Capture Arms the scope for a signal capture.

TV Capture Captures the selected TV line.

Capture & Repeat Arms the scope for a signal capture and automatically applies previously used post-storage functions.

POST-STORAGE FUNCTIONS
CH1 x CH2: Displays (CH1 x CH2)/5.01

CH1 + CH2: Displays the addition of the two signals.

CH2 – CH1: Displays the difference between the two signals.

CH1 – CH2: Displays the difference between the two signals.

(datum referred to centre line of screen)

Copy CH1 – CH2 Copies store 1 to store 2 or store CH2 – CH1 2 to store 1.

Trace Magnification/Attenuation Multiplies trace from x3.98 to X0.06 in 250 steps selectable by step control. Gain is displayed on the screen.

Filter 6 selectable stages of filtering per timebase range.

$$\text{Cut-off frequency} = \frac{8.14}{Tx2^{n-1}} \text{ Hz}$$

Where:- T = Timebase range in s/cm and n = filter stage from 1 to 6.

Invert Inverts trace about the centre line.

Restore Displays trace as if the last post-storage function selected was removed.

Position Moves trace and datum in X and Y planes and cursor in X plane.

ADDITIONAL FACILITIES
Calibrator 1V ±2% square wave approx. 1kHz (approx. 2.3mA to ground).

Z Mod Input DC coupled 2V visible modulation.
Sensivity: +15V cut-off sensitivity.
Impedance: 10kΩ/10pF approx.
Max. input: 100V DC or Pk AC

Ramp Output Nominally + 3.5v ramp from 5kΩ.

NOTE: The fuse ratings marked on the rear panel should be 500mA for 220-240V supply and 1 Amp for 100-120V supply.

Operation

Section 3

INTERNATIONAL SAFETY WARNING
(as required for I.E.C. 248 Class 1)
This instruction manual contains information and warnings which must be observed by the user to ensure safe operation and retain the apparatus in a safe condition. The instrument has been designed for indoor use within the specified limits of temperature. It should not be switched on if there are obvious signs of mechanical damage and it should not be used under wet conditions.

EARTHING
The instrument must be operated with a protective earth connected via the appropriate (yellow/green) conductor of the supply cable. This is connected to the instrument before the line and neutral supply connections when the supply socket is inserted into the plug on the back of the instrument. If the final connection between the instrument and the supply is made elsewhere, the user must ensure earth connection is made before line and neutral.

If any supply cable other then that supplied with the instrument is used, it must carry an adequate protective earth conductor.

Any interruption of the protective earth conductor inside or outside the instrument is likely to make the instrument dangerous. Intentional interruption is prohibited.

Signal connections into the instrument should be connected after and disconnected before the protective earth connection is made, i.e. the supply lead must be connected at all times that signal leads are connected.

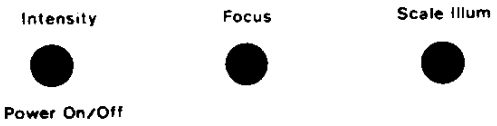
LIVE PARTS
The instrument is safe to operate with the covers fitted and these must not be removed under normal usage. The covers protect the user from live parts and they should be removed only by suitably qualified personnel for maintenance or repair purposes. (see maintenance section).

3.1
Before connecting the 4035 to the supply check that the supply voltage range has been set to suit the supply voltage to be used and that the correct fuse is fitted. The fuse has to be altered when switching between the 100V and 220V ranges. The fuse holder and the voltage switching are both situated behind the cover on the power connector. This cover can only be opened when the power lead is removed.

3.2 OBTAINING A TRACE
To obtain a trace follow the sequence of instructions detailed below:-

1. After connection to the supply, switch on by turning the INTENSITY control clockwise away from the OFF position. Check that the POWER indicator l.e.d. lights.

2. Set to the 'NON STORAGE' operating mode.
MODE switch to CH1.
CH1 Y Position control (vert. arrows) to approx. mid setting.
CH1 VAR SENS control fully clockwise to the CAL position.
CH1 input coupling switch to GND.
Select 'AUTO' trigger (ON).
X10 Position control (horiz. arrows) to approx. mid setting.
TIME/DIV switch to 5μs.
A horizontal trace should appear on the screen as the INTENSITY control is advanced.



3. Adjust the INTENSITY control to obtain a display of the required brightness.
4. Adjust the FOCUS control to obtain a sharply defined trace.
5. Adjust the CH1 Y Position control and the X Position control to centralise the trace on the screen.
6. Adjust the TRACE ROTATE on preset control if necessary to align the trace with the centre graticule line. It may be necessary to re-adjust this control only when the instrument is re-positioned as the beam deflection can be affected by Earth's magnetic field or other sources of magnetic radiation.
7. Switch to a Storage mode (eg Refresh), and select x1 X-expansion. A power up message will appear at the bottom of the screen. This displays the version of the software fitted in the instrument, and the value of the GPIB address, as read from the internal GPIB address switch.

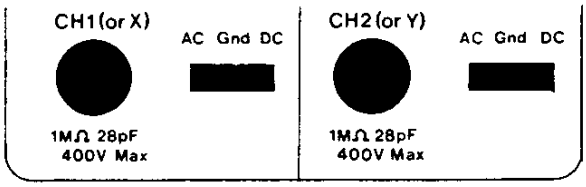
eg. "Vers 1.0 Add = 07"

The presence of this message shows that the initial power-up tests have been successful. Pressing the On/Off cursor button removes this message, and replaces it with the normal cursor measurement display.

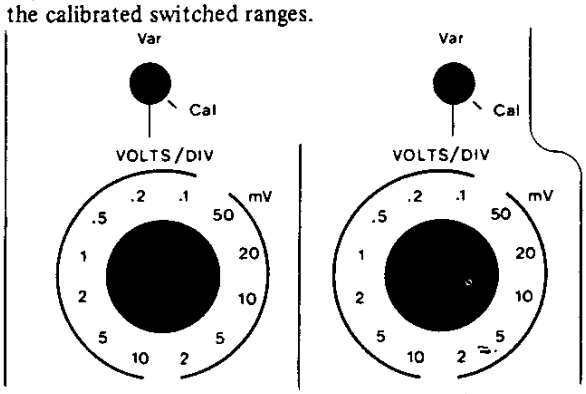
NOTE: THE 4035 SHOULD NOT BE OPERATED CLOSE TO SOURCES OF ALTERNATING MAGNETIC FIELD SUCH AS LARGE TRANSFORMERS AS THESE MAY INTERFERE WITH THE TRACE.
ALLOW 20 MINS FROM SWITCH ON FOR THE INSTRUMENT TO OPERATE TO FULL SPECIFICATION

3.3 CHANNEL 1 & 2

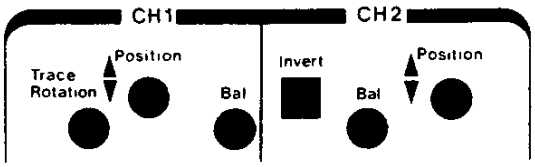
The slide switches AC/GND/DC select the input coupling required. For direct connection of the input signal set the switch to DC, and for capacitive coupling through an internal 0.1μF 400V capacitor set to AC. The input is grounded if the switch is set to GND, the input socket then is open circuit.



The sensitivity of the input channels is selected by the VOLTS/DIV switch. For calibrated operation the VARiable Sensitivity control should be set fully clockwise to the CAL position. However, this control can be used to reduce the gain of the relevant amplifier so that any intermediate sensitivity can be obtained between the calibrated switched ranges.

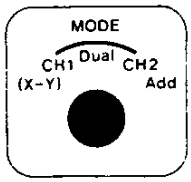


To adjust the position of the trace on the display the POSITION control should be rotated in the appropriate direction indicated by the arrows ▲▼.



3.4 DISPLAY MODES

The mode switch determines the form of the display. Operating as a STORAGE oscilloscope some of the display modes are not available. These will be indicated in the relevant paragraph. The applicable modes are linked with a red line.



3.4.1 SINGLE CHANNEL

For single trace display of one Y input against the timebase the 'MODE' switch should be set to CH1 or CH2 and the input signal applied to the appropriate input connector.

3.4.2 DUAL CHANNEL

For dual trace simultaneous display of both Y inputs against the timebase, the 'MODES' switch should be set to Dual.

In the Non Storage operating mode, two methods are used to display the input signals and are selected automatically by the sweep rate selected by the TIME/DIV switch. The alternate mode is used for fast sweep rates between 0.2ms/div and 0.5μs/div. At the slower rates from 0.2s/div to 0.5ms/div the chop mode operates at approx. 500kHz.

In the STORAGE modes the display is switched alternately at a fixed rate of 200Hz.

3.4.3

In the ADD mode, which is only available in the NON STORAGE operating mode, the single trace displayed is the algebraic sum of the CH1 and CH2 deflections.

If the INV CH2 button is operated the direction of the Y deflection for channel 2 is reversed. If used in conjunction with the ADD mode, the difference between the CH1 and CH2 inputs is displayed. the INV CH2 selection has no effect on the polarity of the internal CH2 trigger.

When examining small differences between large signals, the effect of small errors between the sensitivities of the two channels can be overcome by first connecting one input to both channels simultaneously and adjusting one or other of the Variable and Sensitivity controls to obtain a straight line.

In the STORAGE modes the ADD position of the MODE switch defaults to CH2 operation.

3.4.4 X-Y

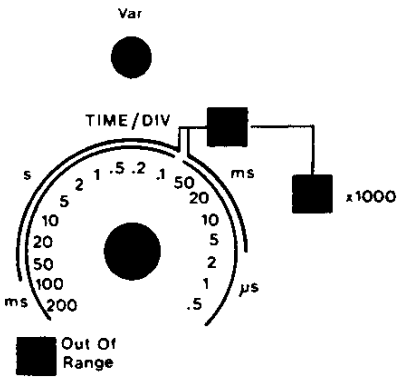
In the X-Y mode, which is only available in the NON STORAGE operating mode, the timebase is disabled and

the CH2 input is displayed as the vertical (Y) deflection against the CH1 input displayed as horizontal (X) deflection. The CH1 shift control is inoperative and X position is determined only the X position control. The X10 MAG facility is also inoperative. X deflection sensitivity is determined by the CH1 controls. The X bandwidth is limited to 1MHz and relative phase shift between X and Y deflections may exceed 3° above 50kHz.

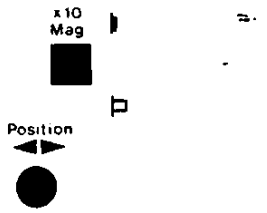
In STORAGE modes selection of X-Y defaults to the CH1 selection.

3.5 TIMEBASE AND X-EXPANSION

The calibrated sweep speed of the internal timebase is determined by the setting of the TIME/DIV switch and is extended in the STORAGE modes by the X1000 (ms–s) button. When this button is in, the milliseconds section of the TIME/DIV switch is converted to seconds, for example 1ms/Div becomes 1s/Div. In the NON STORAGE mode, the sweep rate may be varied by the Variable SWEEP control, enabling intermediate sweep rates between the calibrated ranges to be obtained.

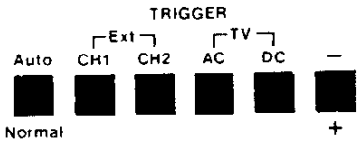


For horizontal trace movement, adjust the X position control (horizontal ◀▶ arrows). If close examination of any portion of the trace is required, X10 expansion can be introduced by operation of the X10 MAG button. This provides an effective trace length of 100cm and any portion of this may be selected for viewing on the screen by operation of the X dual speed position control.



3.6 TRIGGER

The display sweep may be triggered internally from the CH1 or CH2 signals by operation of the appropriate TRIGGER source selection button, irrespective of whether the selected channel is being displayed. Alternatively, the display sweep may be triggered from an external signal applied to the EXT TRIG sockets when both CH1 and CH2 buttons are selected simultaneously.



The +/– button selects the slope, positive or negative going, which causes triggering when the signal passes through the level set by the TRIGGER LEVEL control. Presence of a TRIGGER signal is indicated by the associated TRIGGER l.e.d. This will flash at low trigger repetition rates and remain on at faster rates. Triggering is obtained from internal deflection signals greater than 3mm pk/pk up to 2MHz but the sensitivity reduces above 2MHz to 1-5 div pk/pk at 20MHz. Corresponding external sensitivity is 0.15V pk/pk to 2MHz and 0.6V pk/pk at 20MHz.

With AC coupling, the low frequency sensitivity reduces to 1-5 div pk/pk at about 2Hz.

The Ext Trig input impedance is approx. 100kΩ/10pF and care should be taken not to apply more than 250V d.c. or pk, a.c. to this socket.

When the 'AUTO' button is in, or ON, the timebase will free run in the absence of a correct trigger signal, displaying a bright line or unsynchronised display until the level control is adjusted and/or the amplitude of the trigger signal is increased. The free-run action in the absence of a correct trigger, enables the operator to determine a reference level eg OV. If the timebase is required to free run continuously, the LEVEL control should be set to either end of its rotation.

NORMAL mode must be selected when the instrument is to be used to display signals at repetition rates less than 40Hz or faster than 2MHz preventing additional free-run sweeps from occuring between correctly triggered low frequency sweeps or erratic high frequency operation.

The coupling of the trigger signal may be selected as a.c. or d.c. by operation of the corresponding TRIGGER

coupling buttons. When both are pressed, an active synch. separator circuit is introduced to provide line or frame triggering for video waveforms. Field trigger occurs for sweep rates down to 100μs/div and line trigger is automatically selected for fast sweep rates from 50μs/div. The trigger polarity should be selected for the polarity of the synch. pulses. At least 3mm pk/pk of synch. pulse amplitude is required with internal triggering, or 0.15V with external.

Summarising the use of the trigger controls for most applications:

(a) With AUTO on (button in), select the trigger source CH1, CH2 or EXT and the coupling required, AC or DC.

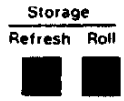
(b) Select the trigger slope + or – and adjust the trigger level control to obtain a trace which is triggered at the required point.

3.7 NON STORAGE

In non storage mode the instrument behaves as a conventional 20MHz oscilloscope is selected by depressing the NON-STORAGE control. All controls associated with the STORAGE mode are disabled.

3.8 STORE CONTROL

The STORAGE mode is selected by operating either the REFRESH or ROLL controls.



3.8.1 REFRESH

Selection of the REFRESH mode produces a display similar to that of a conventional oscilloscope, but the trace is flicker-free even at low sweep rates.

The display updates from the left hand edge of the screen, new information over writing the old. A sweep is initiated by receipt of a trigger, the updated display containing information captured on or after the trigger event. If a trigger is not present the information captured on the previous sweep, will be retained indefinitely until the instrument is rearmed or a trigger occurs.

3.8.2 ROLL

Selection of the ROLL storage mode provides a form of free running trace not found on conventional oscilloscopes. Incoming data is transferred continuously into the display store. As the store receives new data the trace is moved to the left by one store location for each measured data point. As the trace is updated the display appears to be moving or ROLLing to the left, in appearance similar to the view through a 10cm window of a chart recorder.

At any particular moment, T, as data is transferred into the store, the display contains only data captured before time T. If the store trace is allowed to roll a further 2.5div and stopped, the display will contain 75% data captured before time T, and 25% after time T. This is the basis of the PRETRIGGER facility available in the SINGLE CAPTURE mode (and at certain timebase rates in the CONTINUOUS CAPTURE MODE. See 3.8.3, 3.8.6 and 3.8.7).

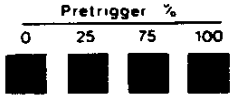
The rate of ROLL is dependent upon the acquisition rate selected by the timebase control and the x1000 button (see section 3.8.8). As the rate of ROLL increases the trace ROLLs across the screen so fast that no useful information can be obtained and so for timebase ranges 0.2ms/Div to 5μs/Div the trace does not ROLL across the screen but is in appearance similar to a "REFRESH" trace, but with the important addition that the trigger point can be in one of four positions across the display (see section 3.8.3). In this mode absence of trigger forces the display to retain the data captured on the previous sweep.

3.8.3 0%, 25%, 75%, 100% PRETRIGGER

Selection of one of these four buttons, in the ROLL mode determines the amount of data displayed before the trigger point.

The amount of PRETRIGGER selected determines the percentage of the displayed data that is required before the trigger point, and hence the position of the trigger point on the display. For example, if a trace is captured, in the SINGLE CAPTURE mode, with 25% pretrigger selected, the trigger point is 2.5 div from the left hand edge of the display the first 2.5 div being PRETRIGGER data and the remaining 7.5 div post-trigger data.

As described earlier PRETRIGGER is only available in the SINGLE CAPTURE mode, but there is an exception. The previous section mentions that at the time-base ranges 0.2ms/div the trace does not ROLL, but the display is updated on the receipt of a trigger and has a "REFRESH" like appearance. In this mode pretrigger is available in the CONTINUOUS CAPTURE mode as well as in the SINGLE CAPTURE mode.



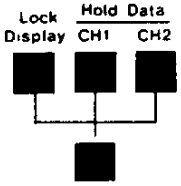
3.8.4 LOCK DISPLAY

Operation of the LOCK DISPLAY button freezes the total display immediately preventing any further data

being written to the display stores. It operates in both the REFRESH and ROLL modes.

In addition to freezing the display, the LOCK DISPLAY control enables the trace to be plotted by operating the MANUAL PLOT 1 or 2 controls. (See section 3.8.9). Operation of LOCK DISPLAY is indicated below the switches.

Releasing the LOCK DISPLAY control forces the capture to resume in the CONTINUOUS mode.



3.8.5 LOCK CH1, CH2

Operation of either of these controls will prevent further data being written into the appropriate memory for that channel. However, the other channels data will continue to be updated unless the LOCK CHANNEL control is also selected for this channel.

A MANUAL PLOT cannot be initiated for the channel whose data is locked (unlike LOCK DISPLAY).

An indication that either of the LOCK CHANNEL controls are in operation is provided by the indicator below the buttons.

Releasing either of these buttons does not effect the capture mode in force at the moment the buttons were operated.

3.8.6 SINGLE CAPTURE

Operation of this button forces the single shot capture mode in which the instrument stores on triggered sweep only and then holds the data until another capture is requested, or the capture mode is altered.

When this momentary action button is operated, the ARMED indicator below will light. The next action depends upon whether REFRESH (a) or ROLL (b) is selected.

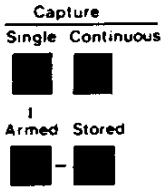
(a) In REFRESH mode the display will not update until a trigger is received at which point data will be stored and displayed from left to right. Once the display is fully refreshed the ARMED indicator will be extinguished and the STORED indicator will light. The display is now frozen and will not alter until another capture is requested.

(b) In ROLL mode the display will begin updating immediately the 4035 is armed. After the store has captured sufficient data to meet the PRETRIGGER requirements, the instrument can accept a trigger. Once a trigger is accepted and the posttrigger data is stored the acquisition will end, at which point the ARMED indicator will extinguish and the STORED indicator will light. The display is now frozen and will not alter until another capture is requested.

3.8.7 CONTINUOUS CAPTURE

Operation of this button selects the CONTINUOUS CAPTURE mode.

In REFRESH mode the display updates for a full timebase sweep and remains. The stored waveform is dis-

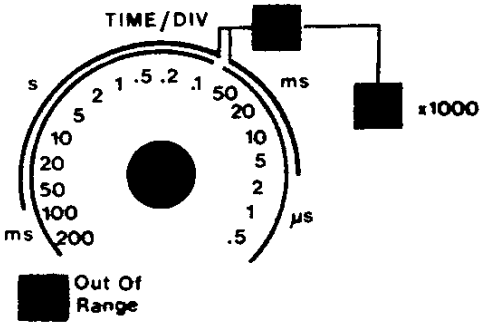


played until another trigger is received, when the display store will begin updating again overwriting the previous waveform.

In ROLL the display rolls continuously ignoring triggers, except at timebase rates 0.2ms/div to 5μs/div as detailed earlier (see section 3.8.2) when a single triggered sweep is captured and displayed on these ranges a trigger is required to update the stored display.

3.8.8 x1000

Operation of the x1000 button multiplies the timebase range by a factor of 1000. For example, if 0.2ms/div is selected and the x1000 button is depressed, the timebase range is now 0.2s/div. The button can only be used in the STORAGE modes and if the timebase range limits are not exceeded. An indicator warns the operator that a timebase range is selected outside limits.



3.8.9. PLOT FACILITIES

There are three types of plot available on the 4035:

Dual analog plot
GPIB digital Talk Only Plot
Auto-Plot

They are controlled by the four front panel buttons Manual Plot CH1 and CH2, and Auto Plot CH1 and

CH2. Operating any of these buttons initiates the plot function. The plot-rate switch on the rear panel determines whether to output in analog or digital GPIB plot. There are eight analog output rate selections. Certain limitations apply to all types of plot. Firstly, plot is only possible in a Storage mode (ie with the Display Mode switch set to either Refresh or Roll). Secondly, plot will only start if a trace is started or locked in display (ie not in Continuous Capture mode). Either by use of the Single Capture button to capture a trace, or use the Lock button to freeze the current trace.

If the trace has not been stored or locked then a warning message will appear on the display.

"NOT ARMED YET"

3.8.9.1 DUAL ANALOG PLOT

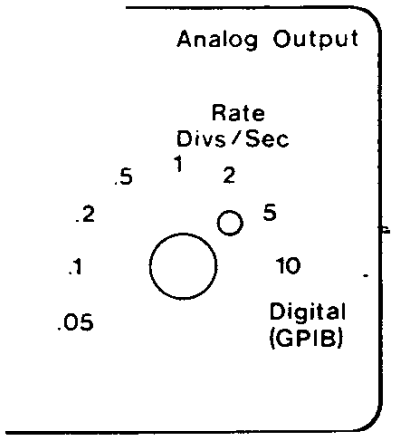
With the plot rate switch set to any position other than the digital plot position, a dual analog plot is started by pushing any of the four plot buttons on the front panel.

Pressing either Manual Plot CH1 or CH2 has the same effect: a simultaneous analog plot is started for each channel.

The outputs are via 4mm sockets on the rear panel, for X, Y1 and Y2, and a penlift signal to control an X-Y recorder pen, or an I-Y recorder motor. Note that it makes no difference which button is pressed, the output for CH1 always comes via the Y1 socket, and the output for CH2 always comes via the Y2 socket.

The required output rate is selected by the PLOT RATE switch on the rear panel, a range of 0.05 Divs/s to 10 Divs/s being provided. The nominal output is 100 mV/Div for X and Y.

NOTE: THE PLOT CAN BE ABORTED AT ANYTIME BY PUSHING EITHER OF THE MANUAL PLOT BUTTONS.



3.8.9.2 GPIB TALK ONLY PLOT

If any of the Plot buttons is pushed when the Plot rate switch is in the GPIB digital plot position, then a digital plot is initiated. This is an output from the GPIB socket on the rear panel in a form suitable for a number of digital plotters with GPIB listen only capability (including Gould and HP plotters). The format used is HPGL, and an example output is shown below (Fig. 12). A box is drawn, with ticks along its edges for calibration. A label at the top shows the attenuator and timebase settings at which the store was captured with a label at each end of the trace. Note that a CH1 digital plot produces its label at the top left, but a CH2 digital plot produces its label at the top right. This means that if CH1 and CH2 are both plotted on the same sheet of paper, the labels are not confused. If the digital plotter used has the capability for different colour pens, a different pen will be used for each channel, so that the two traces can be distinguished. At the end of each plot an overall graticule can be plotted as the full graticule lines (10 DIV x 8 DIV). The alpha numeric display will indicate

"SET DATUM = GRAT"

If not required the next operation of a digital function will cancel the display.

NOTE: THE START OF TRACE IN PLOT WILL ALWAYS BE AT THE LEFT HAND GRATICULE LINE IRRESPECTIVE OF THE X POSITION CONTROL.

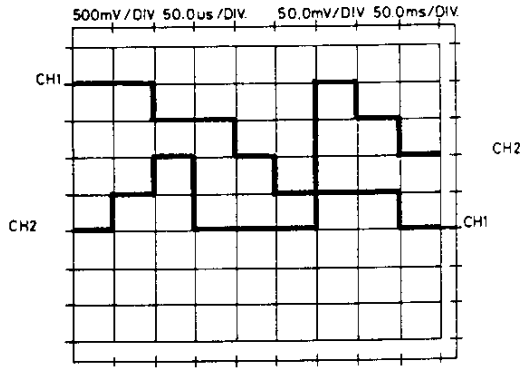


FIG. 12a

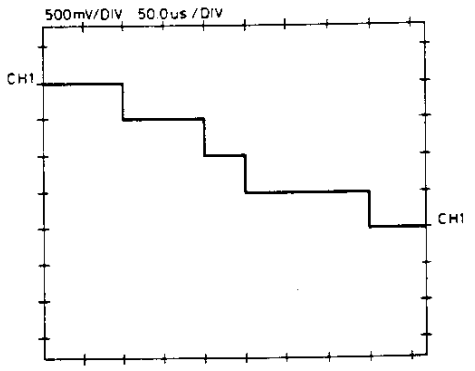


FIG. 12b

3.8.9.3 AUTO PLOT

This facility provides a means of acquiring data then outputting it for plotting automatically. It is known as the baby-sitting mode. It applies equally to analog plot and to digital plot.

To set up this mode, the following sequence should be followed:-

1. Set CONTINUOUS CAPTURE mode.
2. Set up the Y Channel sensitivities, and sweep rate required.
3. Set up the trigger sources level and slope as required.
4. Set up the required plot rate (or select GPIB digital plot)
5. Select either AUTO PLOT 1 OR 2 (note that it makes no difference which is pushed if analog plot has been chosen because both channels are always outputted simultaneously). In digital mode select Auto Plot 1, 2 or both (both will output CH1 then CH2).
6. Select SINGLE CAPTURE mode (Armed).

The instrument will wait for the first trigger, displaying the message

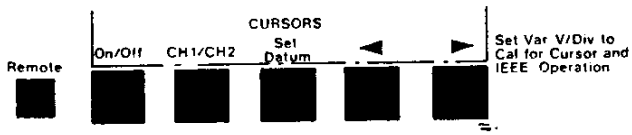
"NOT ARMED YET".

After trigger, the instrument will begin acquiring data. At the end of the acquisition sweep a plotting output cycle will begin automatically and when the process is complete the instrument will be rearmed. A message is displayed, while waiting for the next trigger:

"WAITING FOR TRIG".

When the trigger has arrived, the whole sequence is repeated, until AUTO PLOT is deselected.

NOTE: A PLOT CAN BE ABORTED AT ANYTIME BY PUSHING EITHER OF THE MANUAL PLOT BUTTONS. THE PLOT WILL STOP WHEN THE BUFFER STORE OF THE PLOTTER IS EMPTY.



3.9. CURSOR MEASUREMENTS

3.9.1 THE CURSORS

The measurement system is based around the difference between two samples on a trace. The positions of the two samples are shown on the display by cursors, a small vertical line centred about the trace in question and a datum. the datum is shown by a dotted vertical line the full length of the screen. The main cursor and the datum can be moved to a required position on the trace using the five buttons under the screen. The main cursor can be moved left and right at will, and the datum line stepped to its current position using the Set Datum button. The main cursor can then be repositioned relative to the datum. The display at the bottom of the screen shows the difference between the two sample points on the trace, as pointed to by the main cursor and the datum line.

The buttons are:

On/Off to turn the cursors and the character display on and off.

CH1/CH2 to change the cursors between the traces. Pressing this button moves both cursors from one trace to the other, and the display shows the voltage and time difference between cursors on that trace.

Set Datum Moves the datum line to the current horizontal position of the main cursor. To move the datum line, the procedure is to first move the main cursor to the required psotion, and then push the Set Datum button.

Cursor left/cursor right These two buttons move the main cursor slowly in the required position, and pushing it harder will speed it up by approximately 10 times.

As an additional feature, pushing the On/Off button while the Set Datum Button is already pressed will cause the datum line to move as close as it can to the trigger point on the trace. For example if Roll mode is selected, and Pretrigger is 25%, the datum line will move to a position 1/4 along the trace.

3.9.2 THE DISPLAY

The 16 character display at the bottom of the screen is only visible under certain conditions.

a) The instrument must be in a Storage mode (ie either Refresh or Roll)

b) x10 X-expansion must not be selected.

The display screen consists of 16 characters at the bottom of the screen. As mentioned in section 3.2, a message appears on power up, confirming a successful power up sequence. Pressing one of the cursor buttons removes that message, and the display is dedicated to cursor measurements, showing the voltage and time difference between the main cursor and the datum.

An example of the cursor measurement display is:

"CH1–4.45 V 1.234ms"

As shown the information is in three sections-

channel; voltage difference; and time difference.

The first three characters indicate to which channel the two cursors are allocated, and change between 'CH1" and "CH2" as the CH1/CH2 button is toggled. The next 6 characters show the voltage difference between the

cursors, and the final 7 show the time difference (ignoring decimal points, which do not occupy a character space).

Note that although these numbers might be displayed to several decimal places, the accuracy of the measurement is limited by the digital sampling technique. See the specification section for its actual limits, samples are accurate to 1 in 256 across the screen vertically of 1 in 25 can be expected. The difference between two samples could be in error by 2 bits (1 bit for each sample), giving an accuracy of 1 in 12 for 1cm signal. Horizontal resolution is 1 in 1024 across the screen giving measurements in 0.1/ steps. No account is taken of the Volts variable position therefore the control can be used to scale readings but for full calibration ensure the control is switched to the CAL position.

3.10 GPIB INTERFACE

3.10.1 INTRODUCTION

The interface allows a bus controller to read from and write over the two stored traces, as well as read the state of the front panel buttons, and change a number of them.

A distinction is made between local operation and remote operation, in that when local, the front panel controls the operation of the oscilloscope, and the GPIB can only interrogate the state of the instrument, not alter it. When remote, however, the front panel controls are inactive, the cursors disappear, and the alpha display switches to a display of the state of the GPIB interface. Note that for convenience, an exception is made of the "Single" and "Continuous" capture buttons, which can be used when local or when remote.

An l.e.d. to the left of the cursor buttons ("Remote") indicates when the instrument has gone remote.

When Remote, the cursors are inactive, and the display shows GPIB status information. The cursor buttons are also inactive, except for the On/Off button, next to the Remote l.e.d. If this is pushed, a go to local message is sent to the interface, and if local-lockout is not in action, then the instrument will switch back to local operation.

Service Request is used to indicate errors, as received by the 4035. The value of the service request gives an idea of the type of error received.

When operated without a bus controller, the instrument is capable of sending the contents of either store to a digital plotter in Talk Only mode. The format used is that used by a number of Gould-Bryants and H.P. plotters.

3.10.2 ADDRESS SELECTION

In order to talk to a device, the bus controller must know what address is allocated to the instrument. On the 4035, the GPIB address is selected by a switch inside the instrument. This switch is read infrequently by the instrument. On power up, the switch is read, and its value displayed as part of the power up message (see section 3.2 obtaining a trace). To change the GPIB address, the top cover of the instrument must be removed, and the GPIB address, the top cover of the instrument must be removed, and the GPIB printed circuit board located (to the left of the c.r.t). The address switch is towards the rear of this board, and is labelled "S1". It has 8 switches on it, five set up the address, and three are spare. In the figure below (Fig. 13), the switches shown for GPIB address is 07.

3.10.3 GPIB SYNTAX

A string is the smallest complete message unit.

eg. "HSA=5E-3"

Comma may be used in certain strings as a separator; semi-colon is used to separate strings from each other.

eg. "HSA=5E-3;ST1=1,2,3,4,5,6,7 . . . . . "

A string should contain only ASCII characters (except when sending in binary), and any control characters, or bytes greater than 127, are ignored. Note that spaces in a string are also ignored.

A BLOCK is a collection of strings. It is merely used in to break up bulk transmissions of stores. Blocks are separated by <crlf>. (Carriage return, line feed).

A RECORD A record contains a number of strings or blocks and is terminated by <crlf>. The instrument will accept one record into its input buffer before actioning it (excepting store contents, which will overflow the buffer).

When the instrument transmits, it will issue one record for each interrogative command in the record in the input buffer.

Note that when the 4035 is receiving a record, the correct method of termination is ,crlf>, with EOI asserted with the <lf> can be left out as well, so long as EOI is asserted with the last character of the record. Finally, if <lf> is used to terminate the record, then EOI does not need to be asserted.

So valid record terminators are:

<record>	<crlf>	(with EOI)
<record>	<crlf>	
<record>	<lf>	(with EOI)
<record>	<lf>	
<record>		(with EOI)

EOI signifies to the 4035 that the talker has nothing more to say, so, in the case of multi-record commands (eg. "ST1=. . ."), EOI should be sent only at the end of the last record, otherwise it will signify the end of the command, and no more strings or records will be accepted.

3.10.3.1 OPERATION

The 4035 processed commands sent as ASCII (ISO-7) blocks. The instrument will perform no operations until

a record terminator is received (or the input buffer overflows).

Most commands have an interrogative form, and an assertive form.:

eg. "VM" <crlf> is a request for the current setting to be transmitted

while

"VM-DUAL" <crlf> is a request for the setting to be changed.

Assertive commands can only be sent when the instrument is Remote. If local, then a service request is generated ("Not when Local").

In general, several commands can be combined into a record (each command separated by a semi-colon). The commands will then be actioned in sequence.

eg. "VM=CH1;ARM;STAT"<crlf> will force vertical mode to CH1, arm the scope (equiv to Single Capture), then send the status of the scope. Repeated requests for status could be used to find out when a store had been captured.

There are two exceptions to this rule: the bulk transmission commands ("ST1=. . ." and "ST2= . . . ") must be the last command in a record. This also applies to the special command "ALL".

3.10.3.2 NUMBERS

Commands that have numeric parameters (eg HSA, horizontal speed) require the number to conform to certain limitations:

1. The number must contain less than 20 characters
2. The number must NOT contain a decimal point (ie it must be an integer).
3. The number can contain, but need not contain a sign ("+" or "–")
4. The number can contain, but need not contain an exponent.
5. The exponent is prefixed by "E".
6. The exponent can contain, but need not contain a sign.
7. The exponent must not contain a decimal point.

Note that bulk data transfer commands (eg "ST1") have more strict syntax requirements. See section 3.10.6.

When the 4035 transmits a number, it will conform to the above requirements, but in addition, the mantissa will be less than 4 digits, and the exponent, if any, will be a multiple of 3, eg "HSA=500E-3".

3.10.4 THE DISPLAY WHEN REMOTE

When the instrument goes remote (at the request of the bus controller) the 16 character display that normally displays the cursor difference measurement, is reallocated to displaying the GPIB status.

Note that the display has the same limitations mentioned in section 3.9.2. That it is not available in Normal mode, only in Refresh and Roll modes, and it is not available with x10 X-expansion.

The display has a number of fields:

The first word is always "REMOTE".

If local lockout has been selected, then the word "LLO" follows.

The final Three fields are each one letter fields, and, in order say:

(a) If the instrument is Talker active, Listener active, or neither.

(b) If the instrument is Busy (ie in the process of actioning a command).

(c) If the instrument has generated a Service request that has not yet been serviced.

Some examples of a display are:

"REMOTE LLO TBS"	ie local lockout, talker active, busy, waiting for a serial poll.
"REMOTE "	ie remote, inactive
"REMOTE LB "	ie, listener active, still actioning a command (probably a command that requires more input from the bus)

A GPIB command is available to send a text string to the screen (TXT="<string>"). This takes precedence over the normal Remote status display, which can only be restored by going local and then remote again.

3.10.5 THE GPIB COMMAND

The following is a list of the GPIB commands available for the 4035.

ALL

This interrogative command sends out the complete state of the instrument as though all interrogative commands had been sent. Its response is in the form of a number of blocks, separated by <crlf>, with EOI asserted with the final <lf> of the record.

ARM

This assertive command is the remote equivalent of the Single Capture button on the front pannel. Sending this command arms the 4035 trigger circuitry, it waits for the next trigger, and then captures a trace. A service request is generated ("completed") when the trace is captured. If it is not possible to capture a trace (eg because LOCK=ON, or in a non-storage mode), then a different service request ("selection failure") is generated.

eg "ARM" capture a single trace.

BL

This command is used to set the block length to be used when sending the contents of the stores (ie ST1 and ST2). Its initial value is 0, and it can have a value

between 0 and 80. It specifies the maximum block length that will be sent before sending a <crlf>. The store contents is sent as a list of strings, separated by commas. If the number of characters so far sent is going to exceed the block length, then <crlf> is sent instead of a comma. If block length = 0, then an infinite block length is assumed, and the only <crlf> sent is the one right at the end of the record.

eg "BL"
"BL=0" (4035 response: block length is 0)
eg "BL=32" set the block length to 32.

DPLOT1 and DPLOT2

These commands are the direct equivalents of the GPIB digital plot facilities on the front panel. The response is to send a string for use by a GPIB digital plotter, in HPGL format. The string is extremely long (approximately 8000 characters), and specifies the position of each of the points on the display in terms of its X and Y co-ordinates. See section 3.8.9.2.

Note that because of the GPIB interface ignores whether the Y-Variable controls are in the CAL or the UNCAL state, it is up to the operator to ensure that those controls are in the correct position if a calibrated plot is required.

For reference, a possible first 300 characters of a typical output are shown below:

eg "DPLOT1" send out a digital plot string.

(4035 response:)
SP1;SC-2,1024,-130,+133;PU;PA-1,128;PD.PA1024,128,
1024,-129,819,-129;XT.PA614,-129;XT.PA410,-129;
XT.PA205,-129;XT.PA-1,-129,-1,-64;YT;PA-1,0;YT;
PA-1,63;YT.PA-1,128;PU;SL.3;PU;PAO,129;LB
200mV/DIV 5.00μs/DIV PU;PA1,-20;PD.PA2,-30,3,
-33,4,-34,5,-34,6,-35,7,-36,6,-35,9,-35,10,-34,11,-35,12,
-35,13,-35 etc., etc.

HELLO

The response to this command is to send a string containing the current version number of the software in the instrument. The string is in the same format as the power up message on the screen, and also contains the GPIB address.

eg "HELLO"
"Vers 1.0 Add=07" (4035 response)

HELP

This command is a request for a list of all available commands. The response is a block containing the currently available commands, separated by semicolons. Interrogative commands are distinguished from assertive ones by having a "=" appended. Note that the block length command does NOT apply to this command, and the only <crlf> sent is right at the end of the record.

eg "HELP"
"HELP;HELLO;ALL;PLOT;DPLOT1;DPLOT2;
VM;VM=;HSA;HSA=;ST1;ST1-;ST2;ST2=;

HOLD1 and HOLD2

These interrogative commands send the state of the Hold CH1 and Hold CH2 switches. There are two possible parameters, "ON" and "OFF".

eg "HOLD1"
"HOLD2=OFF" (4035 response: CH2 not held)

HSA

This command is used to read the current horizontal speed (ie the timebase range). If local, then it reports the position of the timebase switch on the front panel. If remote it reports the timebase range, which could be different if the assertive form of the command has been used to program the timebase.

The assertive form sets the timebase range to be used for all subsequent digital acquisitions. It cannot alter the sweep rate for the non-storage mode.

The units used are seconds/division. Note the limitations on acceptable types of number in section 3.10.2.3.

The range of possible values is 50 to 5E-6, in a 1,2,5 sequence (ie 50s/div to 5μs/div).

eg "HSA"
"HSA=500E-3" (4035 response: t/b range is 0.5 sec/div)
eg "HSA=5E-5" set t/b range to 50μs/div.

LOCK

This command is the equivalent of the Lock Display button on the front panel, and has the effect of freezing the display. In its interrogative form, it says if the display is currently locked or not. Its assertive form is used, when remote to lock and unlock the display.

It has two possible parameters, "ON" and "OFF".

eg "LOCK"
"LOCK=ON" (4035 response: display is locked)

MODE

This command can be used interrogatively, and to a limited extent assertively. It can be used to find out if the 4035 is in its non-storage mode, or which of its two storage modes it is in. Thus it has three possible parameters "NORM", "REFR" and "ROLL". As an assertive command it is overridden by the front panel switch, if that switch indicates Non-Storage. It cannot be used to change the mode to Non-Storage.

eg "MODE"
"MODE=REFR" (4035 response: in refreshed storage mode)
eg "MODE"
"MODE=NORM" (4035 response: in non-storage mode)
eg "MODE=ROLL" set mode to roll, storage. (Has no effect in front panel switch says Non-Storage).

NB

This is the Numeric Base command. It is used to set the format to be used by the interrogative form of the "ST1" and "ST2" commands. It has four possible parameters

"BIN", "OCT", "HEX" and "DEC". For more information, see section 3.10.6 Sending and Receiving Stores.

eg "NB=BIN" set numeric base to binary.
eg "NB"
"NB=BIN" (4035 response: base is binary)

PT
This is the Pretrigger command. It is used to set or read the pretrigger value, in the same way as the front panel control. It has four possible parameters, "0%", "25%", "75%" and "100%".

eg "PT" what is the pretrigger value?
"PT=75%" (4035 response: it is 75% pretrigger)
eg "PT=0%" set it to 0% pretrigger.

PLOT
This assertive command initiates a dual analog plot, like the front panel buttons. In the same way, it requires a captured or locked trace before it will operate (use "ARM" or "LOCK=ON"). If the trace is not stable, a service request will be issued ("Selection Failure"), and no plot will be started. While plot is in progress, no GPIB activity is possible, and the alpha-numeric display is not visible. When the plot is finished, a service request is generated ("Completed"). The plot output is from the three 4mm sockets on the back panel. See section 3.8.9.

eg "PLOT" initiate a dual analog plot.
Then wait for a service request to be generated, to signify end of plot.

PR
This is the Plot Rate command. It is used to set or to read the current plot rate, which will be used at the next dual analog plot. The units are Sec/Div. It is equivalent to the plot rate switch on the back panel, when that switch is not in the GPIB digital Plot position (see "DEPLOT1" for digital plot). See also "PLOT" and "RP". If the back panel switch is in the Digital plot position, then plot rate is read as PR=0E+0.

eg "PR" at what rate would the next analog plot be?
"PR=100E-3" (4035 response: it would be 100 ms/div)
eg "PR=2E-1" Well, change it to 200 ms/div.

RP
This is the Rate of Plot command. It is in fact the same as the "PR" command, and can be used equally in the same situations. The difference is that the units used are Div/Sec, the same units as on the back panel.

eg "RP" at what rate would the next analog plot be?
"RP=10E+0" (4035 response: it would be 10 Divs/second, in other words 100ms/div)
eg "RP=5" Well, change it to 5 divisions/sec, ie 200ms/div.

REL
This assertive command is the equivalent to the Continuous Capture button. Sending it releases the trigger circuit, so that it can keep capturing stores, each time it sees a trigger signal.

eg "REL" keep capturing, continuously.

SRQV
This is the Service Request Value command. It is made available for GPIB bus controllers that have no Serial Poll facility. In response to this command. a value of 0 is given if no service requests are stacked up. Otherwise, a number (in decimal) corresponding to the Service Request first in the stack is given. Repeated use of this command will remove SRQ's from the stack. See section 3.10.7 Service Requests.

eg "SRQV;SRQV;SRQV; send out the first three
"SRQV=96" SRQ values (4035 re-
"SRQV=102" sponse: there were 2
"SRQV=0" SRQ's waiting, one for invalid command, one for syntax error)

ST1 and ST2
These are the block transfer commands for sending and receiving the contents of the display stores. They only work in the Storage modes. They send or receive a series of 1022 values in a number of different bases. See section 3.10.7 for more details.

ST1HS and ST2HS
These interrogative commands have the horizontal speed at which store 1 or store 2 were recorded. They are in the same form as the 'HSA' command. Note that the speed for store 1 could be different from the current timebase range if the store was captured a while ago. The units are sec/div.

eg "ST2HS" what was the t/b range, when store 2 was captured?
"ST2HS=200E-6" (4035 response: it was 200μs/div)

ST1VS and ST2VS
These interrogative commands specify the vertical range (ie attenuator setting) at which the relevant stores were captured. They have the same form as the "VS1" and "VS2" commands. The units are Volts/div.

eg "ST1VS" what was the attenuator setting when store 1 was captured?
"ST1VS=5E+0" (4035 response: it was 5 volts/div).

STAT
This is an interrogative command to find out the state of the stores. It has three possible parameters, "ARMD", "RELD" and "STRD". It corresponds to the l.e.d's on the front panel, "Armed" and "Stored". If in continuous capture mode, the response will be "RELD". If the oscilloscope has just been ARMed, it will say "ARMED". When a store-full is finally received it will say "STRD".

eg "STAT" what is the status?
"STAT=STRD" (4035 response: a single trace has been captured.)

TXT

This is a method of putting a message onto the 16 character display. The syntax required is:

TXT="<string>"
or TXT='<string>'

The string should not be more than 16 characters long, though decimal points do not occupy a space. There is only a limited character set available. Basically, only upper-case letters and numbers 0 to 9 are usable, but a number of other characters have had to be added, including +,-,=,a,b,c,d,e,f,r,s, a micro symbol (value hexadecimal 7D).

eg "TXT=' SWITCH CH1 to 5V/DIV' "

VM

This is the Vertical Mode command. It corresponds to the MODE switch on the front panel, and is used to specify which traces are to be displayed. It has three possible parameters, "CH1", "CH2" and "DUAL". The assertive form only works in the Storage modes (Refresh and Roll).

eg "MODE"
"MODE=DUAL" (4035 response: both channels being displayed)
eg "MODE=CH2" display only CH2.

VS1 and VS2

These interrogative commands specify the vertical scaling (ie the CH1 and CH2 attenuator ranges). The units are Volts/Div, and they take no account of either the invert switch, or the Variable gain control.

eg "VS1" what is the CH1 attenuator position?
"VS1=10E-3" (4035 response: it is 100mV/Div)

3.10.6 SENDING AND RECEIVING STORES

This is an extended description of the various commands and formats available when sending store information to, and receiving store information from the 4035. It does not include the DPLOT1 or DPLOT2 commands.

The format used for sending store contents is the same as for receiving. So a record previously read from the 4035 can later be sent back, without modification, to restore the display to its original state. However, ensure that data is not being captured while sending a store to the instrument, or the information received will be immediately corrupted (eg send "LOCK=ON" before sending the "ST1= . . . ." command).

When the instrument outputs mass data, the numeric base and the block length will be as specified in separate commands by the user (ie "NB=" and "BL=").

When mass data is sent to the instrument, the numeric base is deduced from the data string, and the block length is irrelevant.

If the instrument is sent EOI–true with a data byte, the instrument will consider the transfer terminated at that point.

MASS DATA TRANSFER DATA FORMAT

Mass data consists of three main sections:

1. A header which is specific to the command in operation (ie "ST1=" or "ST2=").
2. A numeric base identifier (where appropriate):
   ie #B for binary
   #0 for octal
   #H for hexadecimal
   If there is no identifier, the base must be decimal.
3. The data itself.
   The data represents a value between -128 and +127 (when numeric base is decimal, or between 0 and 255 for other numeric bases). -128 is below the bottom of the screen, 0 is the middle of the screen, and +127 is above the top of the screen. The nominal step size is 0.035 divisions per step, so to calculate the voltage difference between two samples, ya and yb:

$$\text{Voltage Difference} = (yb\text{-}ya)\ \frac{(\ 35\ )}{(\ 1000\ )}$$

(attenuator range in Volts/div)

The data is sent as 1022 numbers in the appropriate base. Each base will be treated separately, because they each have their own special features.

BINARY

Sending data in this format is the quickest method. The string is 1034 bytes long (including the <crlf>), in the following form:

ST1=#Bllddddddddddddd . . . . . ddddddcc<crlf>

Where:

#B is the binary identifier

ll is a two byte count of the following data, up to and including the two byte checksum. Most significant digit first. So the value of "ll" is hexadecimal 0400 (decimal 1024).

dddd . . ddd are the 8 bit binary digits (value 0 to 255) representing the data.

cc is a two byte checksum of the preceeding data not (including the length "ll". Most significant digit is sent first.

If an invalid length is received, a service request is sent ("length error") and the command is aborted. If the checksum is calculated to be wrong, a service request ("checksum error") is sent, but the store has already been received, so it is not very important.

The following programme in BASIC should build up a string that could be sent to the 4035, so as to display four ramps on the screen.

```
10      DIM AS[1500]
20      C = 0                                   REM INITIAL VALUE OF CHECKSUM
30      A$="ST1=#B"
40      A$=A$ & CHR$(4) & CHR$(0)               REM THE HEADER & IDENTIFIER
50                                              REM AND THE LENGTH
60      FOR I = 0 TO 1021                       REM MAIN LOOP
70      X = I MOD 256                           REM DATA TO BE SENT
80      A$ = A$ & CHR$(X)                       REM APPEND THE DATA
90      C = C + X) MOD 65536                    REM UPDATE THE CHECKSUM
100     NEXT I
110                                             REM END OF MAIN LOOP
120     A$ = A$ & CHRS (C DIV 256)              REM APPEND THE CHECKSUM
130     A$ = A$ & CHRS (C MOD 256)              REM Not really necessary!!
140
150     A$ = A$ & CHRS(13)                      REM APPEND <CRLF>
160     A$ = A$ & CHRS(10)
170
180         REM NOW SEND THE WHOLE OF A$ OVER THE GPIB BUS
```

DECIMAL
A string of variable length is sent. It consists of the header "ST1" or "ST2", followed by 1022 decimal numbers, separated by commas, or <crlf>. The numbers are in the range −128 to +127, producing zero for centre screen, and 127 for the top of the screen. Leading zeros are not output, but are accepted. Leading "+" is not sent, but is accepted. No decimal point is accepted, nor is an exponent field.

Values are normally separated by comma, but <crlf> is substituted if the length of the block would otherwise exceed the block length set by the "BL" command. If Block length is zero (its initial value) then a <crlf> is only sent right at the end of the record. Block length can be used to ensure a neat print out on a printer, or for a computer that can only accept limited length strings.

When receiving the information, the 4035 treats commas and <crlf> as the same. So if necessary, each number could be separated by <crlf>.

OCTAL
A fixed length record is sent (4101 characters, including the <crlf>, if BL=0), consisting of the header "ST1=#0", followed by 1022 three character octal numbers. The numbers are unsigned, in the range 000 to 377, with 000 being the bottom of the screen. The numbers are separated by commas, or <crlf>, as for DECIMAL. Leading zeros are sent, but are not necessary when receiving the data.

HEXADECIMAL
A fixed length record is sent (3077 characters, including the <crlf>, if BL=0), consisting of the header "ST1=#H", followed by 1022 character hexadecimal characters. The numbers are unsigned, in the range 00 to FF, with 00 being the bottom of the screen. The numbers are separated by commas, or <crlf>, as for DECIMAL. Leading zeros are sent, but are not necessary when receiving the data.

3.10.7 SERVICE REQUESTS

Service requests (SRQ) are generated by the 4035, to notify the bus controller that certain situations have occurred. They do not in themselves affect the instrument. They can be interrogated by either performing a serial poll on the 4035, or sending the interrogative command "SRQV". In either case the result is a number depending on the reason for the service request. Up to 10 SRQ's can be stacked up, and then pulled off the stack by repeated serial polling.

The following is a list of SRQ values:

SRQ value	Meaning
0	ok
74	completed
96	invalid command
98	SRQ stack overflow
99	buffer overflow
100	selection failure
101	not allowed when local
102	syntax error
103	number out of range
104	length error (for "ST1=")
105	checksum error (ST1=")

3.10.8. GPIB COMMAND SUMMARY

There follows an alphabetical list of available commands, and a brief description of their use.

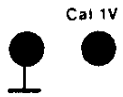
Command	Parameter	Comments	interrog form	assertive form
ALL		status summary	yes	
ARM		single capture		yes
BL	<number>	block length	yes	yes
DPLOT1 DPLOT2		digital plot	no	yes
HELLO		version number	yes	
HELP		list of commands	yes	
HOLD1	ON	lock ch1	yes	no
HOLD2	OFF	lock ch2	yes	no
HSA	<number>	horizontal speed	yes	yes
LOCK	ON OFF	lock display	yes	yes
MODE	NORM	display mode	yes	no
	REFR		yes	yes
	ROLL		yes	yes
NB	<number>	numberic base	yes	yes
PR	<number>	plot rate (div/sec)	yes	yes
PLOT		analogue dual plot	no	yes
REL		continuous capture	no	yes
RP	<number>	plot rate (sec/div)	yes	yes
PT	0%	pretrigger value	yes	yes
	25%			
	75%			
	100%			
SRQV	<number>	service request value	yes	no
STAT	ARMD	store status	yes	no
	STRD			
	RELD			
ST1	depends on	store contents	yes	yes
ST2	"NB" & "BL"			
ST1HS	<number>	st1 horiz speed	yes	no
ST1VS	<number>	st1 vert scaling	yes	no
ST2VS	<number>	st2 horiz speed	yes	no
ST2VS	<number>	st2 vert scaling	yes	no
TEST	WRITE READ LINES PORTS	various test facilities	no	yes
TXT	'<string>'	display a string	no	yes
	or "<string>"			
VM	CH1 CH2 DUAL	vertical mode	yes	yes
VS1	<number>	ch1 attenuator	yes	no
VS2	<number>	ch2	yes	no

3.11 ADDITIONAL FACILITIES

1. Calibrator

The output pin on the front panel provides a positive going 1V flat topped squarewave at approx. 1kHz. It can be used to check the sensitivity of the instrument or to obtain any particular calibrated sensitivity (see section 3.3.4). The rise time is 2μs approx. and the output impedance is 470R providing 2.3mA approx. to ground.

The CAL output may be used to set up passive probes.



2. Z Mod

The socket on the rear panel allows modulation of the brightness. The input is d.c. coupled into approx. 10k/10pF. The sensitivity at normal brightness setting requires approximately 2V to provide visible modulation. 15V is required to obtain a full trace blanking.

Care should be taken not to apply more than 100v d.c. or pk a.c. to this socket.

3. Ramp out

The output of this socket on the rear panel provides a pick off for the ramp which drives the X plates or the c.r.t. In NON-STORAGE mode the duration of the ramp is set by the Time/div control, and is approx. 11 times the range selected. In the STORAGE mode the ramp is fixed at 5ms duration, which is the digital display read out rate. In both cases the amplitude of the ramp is approximately 3.5V, and the output impedance is 4K7.

4. External Control

The digital I/O Connections are provided on a 15 way D type connector on the rear panel providing the following facilities:

(a) External Arm. The instrument may be armed by an external signal. The External Arm Enable must be taken high, 10μs duration (a positive going signal) to the instrument. The input levels are standard Cmos levels 5V amplitude.

(b) Master Arm Out and Master Clock Out. The Arm and acquisition clock signals are provided to enable another instrument to be slaved to the master instrument. The outputs are TTL and CMOS compatible and can drive 6 LS TTL loads (5V).

(c) Slave Enable. If the slave enable signal is taken high the instrument is under control of the Master Arm In and the Master Clock In inputs, and another instrument can Arm this instrument and determine the acquisition rate. In the slave mode the instrument is armed by taking the Master Arm In input high for a minimum of 10μs, and the acquisition rate is determined by the rate of positive going clock edges applied to the Master Clock In input. In this mode the acquisition is always completed before the new data is displayed, so if an acquisition rate of 50s/div is the input from another instrument, the display will not update for 500 seconds after the ARM.

The absolute maximum clock input frequency is 9MHz and the minimum length of a low or high period of the clock must be 55ns.

The inputs are TTL or CMOS compatible (5V and present a load of 4K7 ohms.

(d) Acquisition Gate. This signal is taken low at the beginning of an acquisition. If 0%, 25% or 75% PRE-TRIGGER is selected the acquisition gate goes high when a trigger can be accepted. The Gate signal can be used to trigger another instrument via the External Trigger Input so that the acquisition sweeps are locked together. However, the slave instrument must have 0% PRETRIGGER selected. The output is TTL and CMOS compatible (5V) and can drive 6 LS TTL loads.

(e) Penlift, Plot Y and Plot X Out. The Penlift signal is provided by a pair of relay contacts which close to command a plotter to put its pen down. The Plot Y and Plot X signals are the same as the Plot signals on the 4mm sockets on the rear panel.

Name	D type Pin No.	Type of Input/Output
EXT ARM ENABLE	9	5V CMOS input 10K Pull down.
EXT ARM	1	5V CMOS input 10KΩ Pull down.
$\overline{\text{ACQ gate}}$	10	TTL output
MASTER ARM IN	11	5V CMOS OUTPUT
MASTER ARM OUT	12	5V CMOS OUTPUT
EXT CLK IN	13	5V CMOS COMPATIBLE With pull up.
EXT CLK OUT	6	LS TTL OUTPUT (TO DRIVE SLAVE INSTRUMENT)
GND	14	OV output.
Slave ENABLE	5	LS TTL INPUT 5V CMOS with pull down. COMPATIBLE
Pen Lift 1	3	SHORT TOGETHER for PEN lift during Plot
Pen Lift 2	2	
PLOT Y – CH1	7	Y PLOT OUTPUT see section 4.16
PLOT X	15	X PLOT OUTPUT see section 4.16
PLOT Y – CH2	8	Y PLOT OUTPUT
+5VOLTS	4	see section 4.16

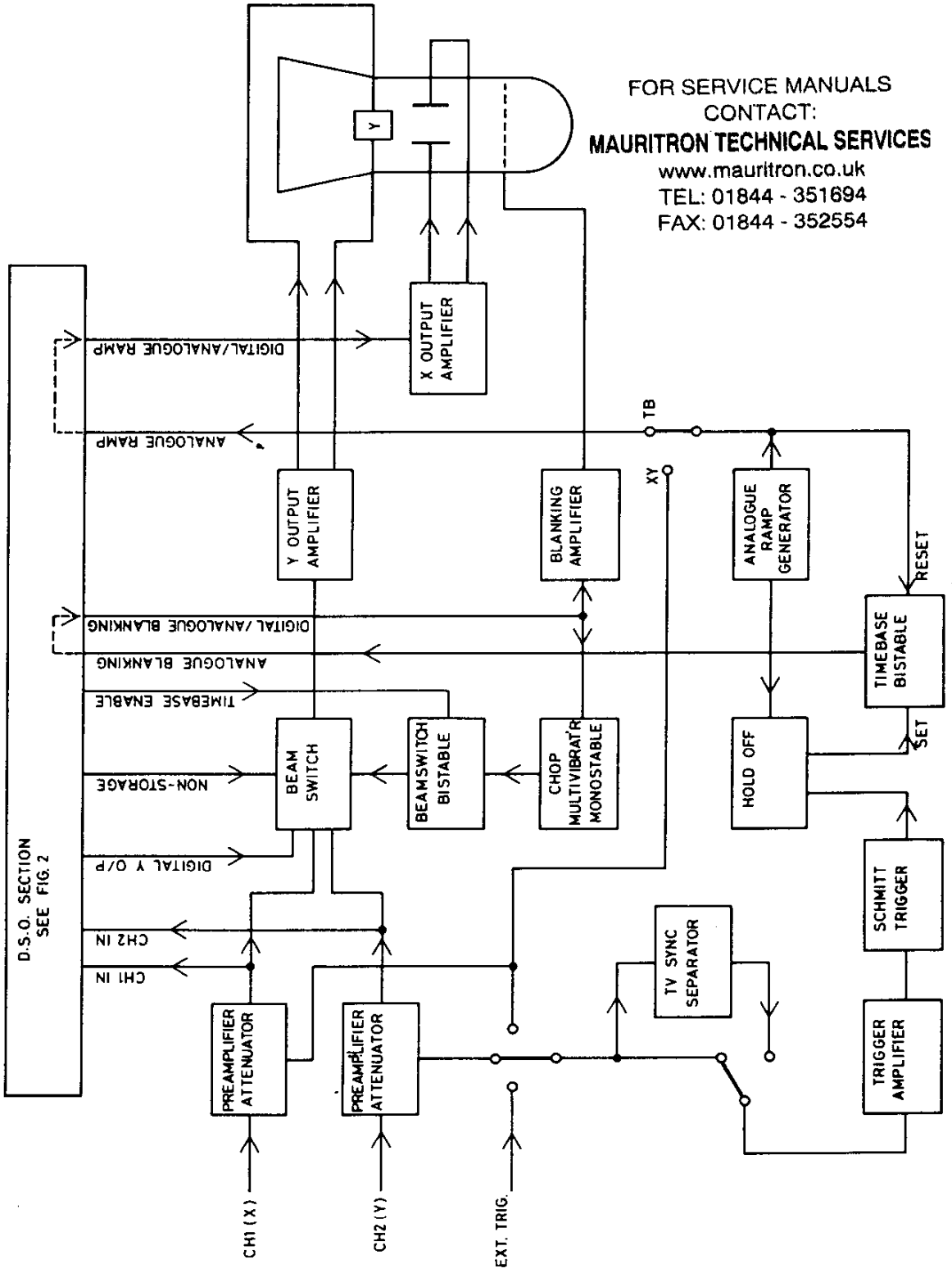


Fig. 1. Block Diagram for 4035 Non-storage

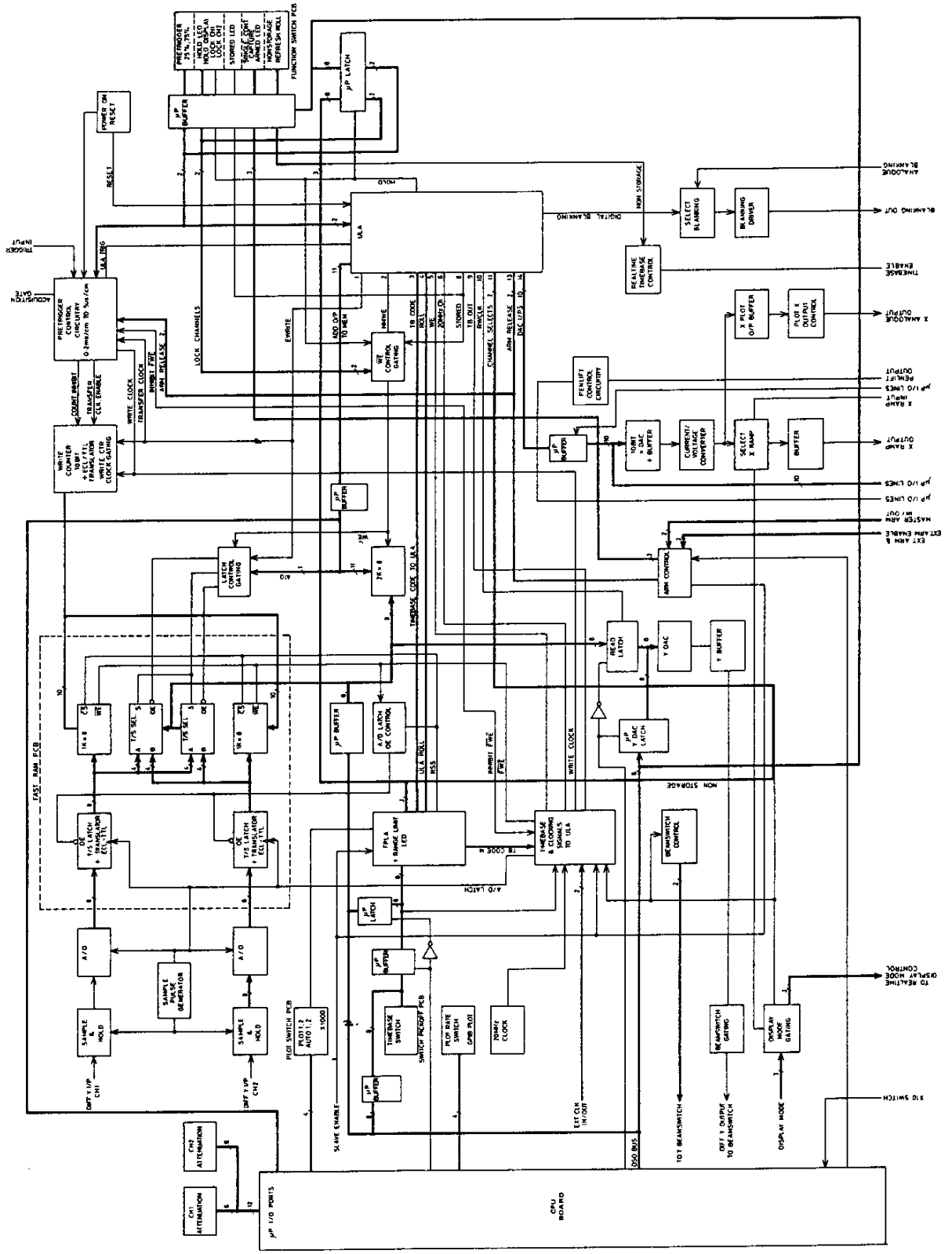


Fig. 2. Block Diagram for 4035 CPU Board

4.1 GENERAL

With the NON-STORAGE control operated the instrument behaves as a conventional oscilloscope. Referring to the block diagram (Fig. 1) signals applied to the CH1 and CH2 input sockets pass into their respective attenuators and amplifiers. The Volts/Div switch controls the gain of the pre-amplifier and the gain of attenuator assemblies to cover a range of input sensitivities 2mV/Div to 10V/Div.

The Variable Gain control adjusts the amplifier gain to give 1 to 2.5 times reduction of gain on all settings of the Volts/Div switch. The fast electronic beam switch selects either CH1 or CH2 signal to be applied further and passed to the Y deflection plates of the c.r.t.

A sample of each signal is taken and passed to the trigger switch bank where selection of CH1, CH2 or Ext trig source is made.

The selected signal is amplified and passed to the Schmitt trigger, the output of which clocks the timebase bistable "on". The ramp generator then begins to generate its linear ramp, which, after passing through the X amplifier, is applied to the X deflection plates of the c.r.t. and drives the electron beam across the tube face. A portion of the signal from the ramp generator is fed back to the hold-off circuit, shutting the gate to prevent any further pulses from the Schmitt trigger from reaching the timebase bistable during the ramp period. When the ramp has reached the necessary maximum level, the timebase bistable is reset, and the ramp is quickly returned to its quiescent state. A time-constant in the hold-off circuit retains this signal to inhibit another ramp from being initiated for a short period, until the ramp timing capacitor is discharged fully. Thus a ramp is generated at a rate set by the TIME/DIV switch when the trigger signal reaches a pre-determined level. This ramp sweep the beam across the c.r.t. face, returns and waits for the next input cycle to reach the set trigger point, so producing subsequent ramps. The timebase bistable is connected to a blanking amplifier whose function is to turn on the electron beam during the sweep and blank it off during the fly-back and subsequent waiting period.

At fast sweep rates for a dual trace display, the TIME/DIV switch automatically selects the alternate sweep mode of control for the beam switch. At the end of each sweep, the signal from the timebase reverses the state of the beam switch bistable, causing alternate displays of the CH1 and CH2 signal on successive sweeps of the timebase. At slow Sweep rates, the chop mode is selected, when the chop multivibrator free runs independently, causing the beam to switch or chop between CH1 and CH2 levels during the sweep.

A signal from the multivibrator also blanks the trace during each switching transition. With CH1 or CH2 only selected, the beam switch bistable is held to select that channel only. In the X-Y mode, the bistable is held to select CH2 as the Y deflection signal, while an additional switch diverts the output from the CH1 pre-amplifier to the X output amplifier, as the X deflection signal in place of the normal ramp signal. The blanking amplifier is held in the bright-up state. When TV trigger mode is selected, an additional sync. separator circuit is introduced into the signal path leading into the trigger amplifier.

When either the ROLL or REFRESH controls are operated the instrument goes into the digital storage mode.

Analogue signals from the Y preamplifier are picked off. buffered and fed into two Sample and Hold circuits. The outputs of the Sample and Hold drive the two 8 bit Analogue to Digital Converters. These produce two eight bit Words representing the instantaneous amplitude of the signal inputs, from CH1 and CH2, at 50ns intervals. The data produced is loaded into either the Fast Store or the Display Store directly, but only 1 in n data samples are stored depending upon the required acquisition rate.

The rate at which data is stored is defined by a programmable digital divider which divides the 20MHz clock under control of the TIME/DIV switch so that 100 samples per div are obtained. Expansion of the display is carried out in the X amplifier and gives a resolution of 10 samples/div.

If necessary data is transferred from the Fast Store into the Display Store. This data is then read out (non destructively) at a fixed rate and reconstructed as an analogue signal by the Digital to Analogue Converter (DAC), and applied to the Y output to give a continuous display of the store contents. Since the output of the DAC is in the form of discrete levels a dot joiner is included to join these levels and provide a continuous display.

In the two digital storage modes the timebase sweep is controlled by a ten bit counter which provides an increasing ten bit code which is reconstructed by a ten bit DAC and dot joiner to give an analogue ramp. This ramp is synchronised to the readout of the Y data from the store. This ramp is used to display the two sections of 1024 bytes of store alternately, or just one section if in a single channel mode, the lower 1024 bytes CH2 information. The trigger is now entirely dissociated from the timebase since the latter runs continuously. The function of the trigger now is, in REFRESH to initiate a write cycle. during which a screen full of new information is entered into the store, and in ROLL to define the amount of pretrigger and post trigger information held in the store.

When the cursors are selected a further display slot is introduced, this includes the two cursors and the line of alpha-numeric text. The microprocessor repeatedly reads the position of the cursors from the display store and shows their difference in voltage and time on this line of text.

4.2 THE Y AMPLIFIERS AND BEAMSWITCH

These circuits are shown in Fig. 21 and Fig. 22. The attenuators and preamplifiers of Channel 1 are identical to those of Channel 2, accordingly only Channel 1 is described.

The input signal is applied to SKA and then to the attenuator via the three position slide switch, S101. This allows the input to be directly coupled through in the DC position or coupled via C105 in the AC position. In the central GND position the input signal is left open circuited while the input to the attenuator is grounded.

On the most sensitive ranges, 2mV/div to 100mV/div, the Volts/div switch S102 couples the signal directly to the preamplifier, the input impedance being defined by R204. On the ranges 0.2V/div to 1V/div S102 introduces N101d and N101c into the signal path to provide an attenuation of 10:1 High frequency compensation of the attenuator on these ranges is provided by C109 and C104, while C101 and C102 allow the input capacitance to be set up to match that on the unattenuated ranges. On the ranges 2V/div to 10V/div S102 introduces N101b and N101a into the signal path to provide an attenuation of 100:1 High frequency compensation of the attenuators is provided by C108 and C107 while C110 and C106 allow the input capacitance to be set up to match that of the unattenuated ranges.

Diode D202 with R205 provide input protection by limiting the negative input voltage to the voltage of zener diode D201.

The input stage of the preamplifier is formed by the f.e.t. source followers U201a and U201b, and the emitter followers U202a and U202b. Imbalance in this stage is corrected by the ATTEN BAL control potentiometer R301.

The differential output from the emitter followers U202a and U202b is tapped off via a constant impedance resistor network N201 which produces an attenuation of 20, 10, 4, 2 or 1. When 2mV/div or 5mV/div is chosen S201, which is the second wafer on the Volts/div switch selects the output which has an attenuation of 1, and if 10mV/div is chosen S201 selects an attenuation of 2. For the ranges 20mV/div to 10V/div, as the Volts/div switch is rotated S201 selects attenuations of 4,10, 20 in turn, the sequence repeating three times.

The tapped signal is amplified by the amplifier consisting of U202c and U202d. The VARiable gain control R213 increases the attenuation of the tapped signal into this amplifier, providing an adjustment of the overall sensitivity of the preamplifier. At this stage, on the 2mV/div range of the Volts/div switch S201 connects R211 and C205 across the emitters of U202c and U202d, increasing the gain of this stage by a factor of 2.5 R215 provides an adjustment which ensures the amplifier is balanced correctly at the 2mV/div range.

The differential signal from U202c and U202d is amplified further by the amplifying stage U301d and U301c. The gain of this stage, and of the preamplifier overall, is controlled by the preset potentiometer R302 and R309 which shunts the emitters of U301d and U301c. The differential output is balanced by the bias through R214 from preset R215, and buffered by the emitter followers U301a and U301b.

The output of the preamplifier is split. The signals are fed to the Analogue to Digital converter (see section 4.9) and, via R316, R317 to the beamswitch. The Y shift currents from the CH1 position control R315, defined by R318 and R319, are summed into the beamswitch also. As mentioned earlier the circuitry of CH2 is identical to that of CH1, but at this point there is one slight difference. CH2 has an invert switch S301 which reverses the output of the preamplifier in the INVERT mode.

The signal currents from CH1 and CH2 are fed into a three way beamswitch with the signal from the digital reconstruction circuitry (See section 4.14). The beamswitch is formed by diodes.

D301, D302, D303, D304, D351, D352, D353, D354, D826, D827, D828 and D829. In NON STORAGE mode the output of inverter U886b is low switching off Q530 and Q531, and taking low the junction of D826 and D828 which diverts the signal currents from R1000 and R1001, reverse biasing D827 and D829. The junctions of D301, D302 and D351, D352 are then both under the control of U501b. This bistable controls the beamswitching of the two Y channels into the Y output amplifier (See section 4.5 Mode control circuits). In STORAGE mode the output of U886b is high, forcing the junctions of D301, D302 and D351, D352 low via Q530 and Q531, and diverting the Y preamplifier signals from the Y output amplifier. At the same time the junction of D826, D828 is taken high, forward biasing D827 and D829, and gating the signal from the digital reconstruction circuitry to the Y output amplifier.

The input stage of the output amplifier consists of a differential shunt feedback amplifier formed by Q401 and Q402. The outputs of this stage are fed into the grounded emitter amplifier stage Q403 and Q404. This in turn drives the differential cascode Y output stage Q405, Q406, Q407 and Q408 which drive the Y deflection plates of the c.r.t. High frequency compensation of the output amplifier is provided by networks between the emitters of Q403 and Q404 and those of Q405 and Q406. Adjustment of this compensation is by C402 and C405.

4.3 TRIGGER CIRCUITS

These circuits are shown in Figs. 21 and 22.

The Trigger Source switches, S502 and S503, connect the required trigger signal via the Trigger Coupling switches, S504 and S505, to the trigger buffer amplifier formed by TR601 and TR602, S502 selects the differential CH1 signal via R313 and R314 from IC301 (Fig.13). S503 selects the equivalent CH2 signal via

R363 and R364 from IC351. Where both S502 and S503 are selected, both of the above signals are disconnected and the single-sided input from the EXT TRIG input socket SKC is selected.

When the AC coupling switch, S504, is out, the trigger signals are directly coupled-through, but when this switch is in, AC coupling is introduced via C603 and C604 (C601 on External). TR601 and TR602 form a differential buffer amplifier with the DC balance controlled by the TRIGGER LEVEL control, R602. The differential output from this stage is applied to the comparator, IC602, which has positive feedback applied by R623 to form a Schmitt trigger circuit. The change-over switch, S506, reverses the output from T601 and TR602 to determine the trigger slope.

When both S605 and S505 are "in" (AC and DC in for TV mode), the junction of R603 and C610 is connected to the −11V supply, D601 and D608 are brought into conduction while D602 and D604 are reverse biased. This diverts the output of the trigger amplifier away from IC602, into TR605, which amplifies the positive tips of the video waveform only. TR605 is prevented from saturation by feeding back the peak detected synch. pulses via TR607 and TR606 to the emitter of TR605. These pulses are amplified by IC601b and applied via R617 and D603 to the Schmitt trigger, IC602. IC601a is used in conjunction with S504 and S505 to disable the synch. separator when AC or DC is selected.

At the fast timebase sweep speeds, S262a is open and TR603 is cut off. However, at speeds of 100μs/Div and slower, R608 is connected to +11V and TR603 is switched on. This effectively grounds C609 to introduce an RC integrating time constant into the synch. pulse signal time path in the TV mode to separate out frame trigger.

The output of IC602 is used by the timebase generator (see next section.)

4.4 ANALOGUE TIMEBASE GENERATOR & X AMPLIFIER

The squarewave trigger output from IC602 is applied (with d.c. bias of zener diode, D605) as the clock to the D type TTL flip-flop, IC501a. A positive-going trigger edge will clock the bistable driving Q low. In the waiting state. Q was high (+4.5V), turning on TR261 via R507 and R262, holding the input, and hence the output of the operational amplifier, IC261 at OV. This timebase amplifier is connected as a direct voltage follower.

When the trigger signal sends Q of IC501a low, the timebase clamp transistor, TR261, is turned off. Part of the constant current generated by TR264 flows through the resistor network, RN272, to charge C263 at a constant rate. The resultant positive-going linear ramp voltage generated at the input of C261 is buffered by that amplifier to generate the low impedance ramp output.

The timebase range switch, S262, selects the tap point on the network, RN272, to vary the ramp slope in the 1.2.5. sequence over a range of three decades. On all fast sweep ranges, TR262 is biased-off but on ramps 0.5ms/cm and slower, S262c connects R263 to +11V. TR262 is turned on and C264 is effectively connected in parallel with C263 to slow the sweep rate 1000 times.

The constant current into the ramp generator is derived from the current mirror circuit formed by TR262 and TR264. The variable gain control, R261, provides an approximate 3:1 range of variation in this current, R506 provides a preset calibration control on the slow sweep rates, only when S262c is closed.

When the ramp reaches its maximum level the negative bias, introduced by R521 and R519, is overcome and TR503 turns on, driving the reset input of the timebase bistable low. As the bistable switches, Q returns high and TR261 conducts to discharge the timing capacitor(s) and the sweep is complete. However, a hold-off action takes place to inhibit trigger signals during sweep and this remains for a short period after a sweep to ensure that the ramp potential is fully reset before the next sweep can be triggered. As the ramp goes positive, D506 conducts to charge C502, reverse biasing D503 and turning on TR502. At the end of the sweep when the timebase bistable is reset, Q goes low and the D input follows via the action of D508 and D511. The ramp output returns rapidly towards OV but TR502 remains in conduction for a period determined by C502 and R518. Only when TR502 turns off can R516 and D507 take the D input high for the bistable to respond to the next clock input.

TR501 acts in a similar way to TR262 (described above) to introduce additional hold-off time through C501 on the slower half of the timebase ranges.

The bright line facility causes the timebase to free-run in the absence of trigger signals. The squarewave input from the Schmitt trigger, IC602, is coupled via C615 into the peak detector diodes, D606 and D607, to generate a positive going signal into the −ve input of IC601c driving its output negative. In the absence of such trigger signals for a period determined by C618 with R627 and R626, the output of IC601c goes positive. When TR502 turns off at the end of the hold-off period, D509 conducts to turn on TR504, driving the set input low to initiate another sweep.

This free-run condition is removed as soon as IC601c detects an output from the Schmitt trigger. When the o/p of IC601c is low it indicates the presence of a trigger signal lighting Trigger l.e.d. via U873f and U878 Pin 18.

This free run condition can be inhibited by releasing the AUTO switch S501 which takes the junctions of D509 and D505 low via R562.

The output of the ramp generator U261 is fed to the analogue multiplexer U859a on the DSO pcb. The other input to the multiplexer comes from the output of the digital ramp generator (see section 4.15). In the NON

STORAGE mode the ramp output of IC261 is selected, U859a pin 9 being driven low by U886b pin 4. The ramp is then buffered by U860c, a unity gain buffer, and drives the X amplifier in the STORAGE mode the output of the digital ramp generator is selected and as in NON STORAGE mode drives the X amplifier via U860c.

The X output amplifier is formed by the shunt feedback stage of TR509/TR511 driving single sided into the amplifier stage, TR513 and TR514. The collector output of this stage drives the X deflection plates of the c.r.t. directly from TR514 and via emitter follower TR515 and TR513. The gain introduced by TR509/TR511 is defined in the X10 magnification mode by the input resistance, R539 and the feedback resistance R552, with the preset, R553 In this mode the transistor switch, TR512, is biased off. However, in the normal X1 magnification mode S507 is open and the current in R548 turns on TR512, introducing R544 with preset, R511, as additional feedback to reduce the gain of the amplifier accordingly.

The X shift controls R271, and R274 introduce an additional bias via R541, R272, R273, and emitter follower Q506 through the potential divider R569 and R545.

4.5 DISPLAY MODE CONTROL CIRCUITS

The display mode is controlled by S261 (Fig. 22) and the NON STORAGE, ROLL, REFRESH controls.

S261 defines the state of three control lines L1, L2, L3. The state of these three control lines is modified on the DSO pcb to produce the three control lines DL1, DL2, DL3. The gating controlling these lines is U73a, b, c, d, e. U74a, b, c, d, U75a, b, U76a, b, c. The outputs of this gating are level shifted by transistors Q829, Q830 and Q831, and then drive the mode control circuitry.

In NON STORAGE mode the lines DL1, DL2, DL3 follow L1, L2, L3 but in the STORAGE modes these lines behave as shown in the TABLE below.

Section 4.2 described the action of beamswitching diodes. D301 to D304, D351 to D354 and D826 to D829, and as mentioned then in NON STORAGE mode the diodes D301, D302 and D351, D352 are controlled by the outputs of beamswitch bistable, IC501b. In the CH1 mode, DL1 is low allowing R525 to take the set input of the bistable low, Q is high and $\overline{Q}$ is low, selecting the channel 1 signal for Y display. In the CH2 and X-Y modes. DL1 is at +11V and R514 takes the set input high but L2 is open and R524 takes the reset input low to reverse the bistable and select the channel 2 signal.

In the Add mode, both DL1 and DL2 are low so that both set and reset are applied to the bistable, Q and $\overline{Q}$ are high and both channel signals are added into the shunt feedback stage of the Y amplifier (Fig.4). In this mode only, DL1, DL2, and DL3 are open, removing the bias through D401, D402 or D403 and defined by R401 and R402 via D405 and D406. This offsets the additional bias introduced by the selection of both channel signals.

Only in the X-Y mode, DL3 is held at +11V to turn on the diode gate of D515 and D514, so coupling the Channel 1 preamplifier signal of IC301, via TR506 and R547 into the X output amplifier. At the same time

NON STORAGE MODE

							IC501b	
DISPLAY MODE S261	L1	L2	L3	DL1	DL2	DL3	Q	5
X-Y	+11V	0	+11V	+11V	0	+11V	L	H
CH1	0	+11V	0	0	+11V	0	H	L
DUAL	+11V	+11V	0	+11V	+11V	0	SWITCHING	
CH2	+11V	0	0	+11V	0	0	L	H
ADD	0	0	0	0	0	0	H	H

STORAGE MODE

							IC501b	
DISPLAY MODE S261	L1	L2	L3	DL1	DL2	DL3	Q	Q
X-Y	11V	0	+11V	+11V	0	0	L	H
CH1	0	+11V	0	+11V	0	0	L	H
DUAL	+11V	+11V	0	+11V	0	0	L	H
CH2	+11V	0	0	+11V	0	0	L	H
ADD	0	0	0	+11V	0	0	L	H

D504 conducts to turn off the gain switching transistor, TR512 thereby selecting x10 X magnification irrespective of the positive of S506.

D501 conducts allowing current through R509 to turn on TR261, clamping the ramp generator so that no signal is fed into the X amplifier via R539. Finally, current through R512 turns on TR504, holding the timebase bistable set "on" to provide continuous bright-up of the trace.

In the Dual mode, both DL1 and DL2 are held at +11V so that the beam switch bistable, IC501b, is free of set or reset signals. Thus it can respond to clock signals and as its D input is connected to its Q output its state reverses on each clock input.

On the fast sweep ranges (0.2ms/Div and above), the clock input is derived via emitter followers, TR505, directly from the Q output of the timebase bistable. Thus the beam switch operates in the alternate mode. The Y deflection is switched between channels at the end of each sweep. TR507 and TR508 form a free-running emitter coupled multivibrator but on the above ranges, S262f is open such that R534 is disconnected and the multivibrator is disabled.

On the slow ranges (0.5ms/Div and below), R534 is connected to +11V and the multivibrator runs. During each sweep period, the multivibrator provides continuous clock inputs to the beam switch bistable so that the beam deflection signal is made to chop between the two channel signals. The beam switching is inhibited between sweeps as the emitter follower, TR505, clamps high the clock input to the beam switch bistable. In all modes, but Dual, DL1 or DL2 are low and D512 or D513 conducts to inhibit the action of the multivibrator.

IC601d is used for the 1kHz calibrator. It is connected as an oscillator with positive feedback via R629 and negative feedback via R633. This with C617 defines the frequency as approx. 1kHz. The output is buffered by the transistor switch, TR604, which defines the calibrator output amplitude via the potential divider of R638 and R643 with preset, R641.

In the STORAGE mode DL1, DL2, DL3, as shown in the table above, force all selections on S261 to be effectively CH2. The beamswitch bistable, IC501b then behaves as described above for this mode. However, since both outputs from the Y preamplifiers are disabled by $\bar{Q}$530 and Q531, the beamswitch bistable does not control the input to the Y amplifier, and the Y amplifier is driven by the Y DAC.

4.6 FUNCTION SWITCH PCB CIRCUITRY

The Function Switch PCB controls the selection of the following modes:

NON STORAGE. With the button out the NORMAL signal to the DSO PCB is taken low by S1101a, and with the button depressed the NORMAL signal is taken high by R1103.

REFRESH. With the button out the ROLL signal to the DSO PCB is taken high by R1104, and when the button is depressed S1101b takes low the ROLL signal.

ROLL. The ROLL button does not generate directly the ROLL signal but a mechanical interlock forces the REFRESH button to be released if the ROLL button is depressed taking high the ROLL signal. The ROLL button when depressed takes high the junction of R1101 and R1102 which is grounded if REFRESH is selected.

0%, 25%, 75%, 100% PRETRIGGER. These four buttons are interlocked so that only one is depressed at any one time. The four buttons produce two signals PER25 and PER75, but these signals are forced low if REFRESH is selected since the junction of R1101 and R1102 is taken low in REFRESH. If ROLL is selected the signals PER25 and PER75 are as shown in the table below.

	0% PRE-TRIGGER	25% PRE-TRIGGER	75% PRE-TRIGGER	100% PRE-TRIGGER
PER25	LOW	HIGH	LOW	HIGH
PER75	LOW	LOW	HIGH	HIGH

HOLD ALL. With the button out the set input of U1101a is high, the reset input low, taking Qa, which is the HOLD ALL signal, low. If the button is operated the set input is taken low, the reset high, taking high the HOLD ALL signal.

LOCK CH1. With the button out the set input of U1101b is high, the reset input low, taking the HOLD CH1 signal, Qb, low. If the button is operated the set input is taken low, the reset high, taking high the HOLD CH1 signal.

LOCK CH2. With the button out the set input of U1102a is high, the reset input low, taking low the HOLD CH2 signal Qa. If the button is operated the set input is taken low, the reset input high, taking high the HOLD CH2 signal.

SINGLE CAPTURE. With the button out the set input of U1102c is low, the reset input high, taking high the ARM signal, Qc. If this button, which is a momentary action type, is pushed in, the set input is taken high, the reset low, taking low the ARM signal until the button is released.

CONTINUOUS CAPTURE. With the button out the input of U1102b is low, the reset high, taking high the RELease signal from Qb. If the button, which is a momentary action type, is pushed in, the set input is taken high, the reset low, taking low the RELease signal until the button is released.

In addition, the Function Switch PCB contains three l.e.d.s D1101, D1102 and D1103. These are illuminated if the relevant signal from the DSO PCB is taken low.

4.7 PLOT SWITCH PCB CIRCUITRY

The PLOT SWITCH PCB contains the controls which select the following modes. x1000. With the button out the signal x1000 is high due to the action of N101h. if the button is operated S1201a takes low the x1000 signal.

PLOT 1. With this button, a momentary action type, not pushed in, the set input of U1201d is high, the reset low, taking low the PLOT 1 signal from Qd if the button is operated the set input is taken low, the reset input high, taking PLOT 1 high while the button is held in.

PLOT 2. With this button, a momentary action type, not operated, the set input of U1201c is high, the reset low, taking low the PLOT 2 signal from Qc. If the button is pushed in, the set input is taken low, the reset high, taking high the PLOT 2 signal.

AUTOPLOT CH1. With this button out the set input of U1201a is high, the reset low, taking high AUTO 1 from Qa. If the button is operated the set input is taken low, the reset high, taking high the AUTO 1 signal.

AUTOPLOT CH2. With this button out the set input of U1201b is high, the reset input low, taking low the AUTO 2 signal from Qb. If the button is depressed the set input is taken low, the reset high, taking high AUTO 2.

In addition to the switch circuitry the Plot Switch PCB contains four l.e.ds D1201, D1202, D1203 and D1204, which light up if the relevant signal is taken low.

4.8 FAST RAM PCB CIRCUITRY

This circuit is shown in Fig. 24.

This circuit acts as a temporary storage buffer between the Analogue to Digital converters (A.D.C.S) and the display store. This storage facility is only used for data rates in excess of 200k bytes per second. At slower speeds the store is bypassed and data goes directly to the display store.

The data from the A.D.C.S is buffered by U1407 and U1408 for CH1, and U1401 and U1415 for CH2. These I.C.s convert the E.C.L. level signals of the A.D.C.S into T.T.L. compatible ones for the store. The data is then held in the retiming latches U1409 and U1414, the most significant 4 bits of CH1 and CH2 in U1409, and the least significant 4 in U1414. In high speed acquisitions, 0.2ms/Div or faster, the data is stored in the ram formed by U1410, U1411, U1412 and U1413. Each ram holds 1024 x 4 bits, U1410 holds CH1 M.S.B.s, U1413 CH1 L.S.B.s, U1411 CH2 M.S.B.s, and U1412 CH2 L.S.B.s. The address and the $\overline{WE}$ pulses are generated by the fast store control circuitry described in section 4.11. The 10 bit address $\overline{WE}$ and WCLK signals which come from the store control circuit at E.C.L. levels are converted to T.T.L. by U1403, U1404 and U1405.

At the end of an acquisition, 1024 consecutive bytes, the accumulated data is transferred to the display store. The control circuit forces latches U1409 and U1414 to their high impedance state and $\overline{WE}$ is forced high. One byte for each channel is read out of the stores every 5μs and presented to the inputs of the data selectors. The M.S.B.s to U1402 and the L.S.B.s to U1406. The output is controlled by the CH2/$\overline{CH1}$ signal. When low CH1 data is selected, and when high CH2 data is selected. The outputs of U1402 and U1406 go directly to the display store, sharing the bus used by the Y D.A.C. In every 5μs period 2.5μs are allowed for transfer of data and 2.5μs for updating the Y D.A.C. When the D.A.C. is being addressed the data selectors are forced into high impedance by the control signal $\overline{OESEL}$.

For slower acquisitions, 0.5ms/cm and slower, the A.D.C. data is held in latches U1409 and U1414 then presented directly to the data selectors. It is then transferred to the display store as described above. In this way the display is continually updated, rather than only at the end of acquisition.

4.9 ANALOGUE TO DIGITAL CONVERTER

This circuit is shown in Fig. 23.

The operation of CH1 and CH2 Analogue to Digital Converters (A.D.C.s) is identical, hence only CH1 is described.

The differential CH1 Y output is picked off the pre-amplifier as described in Section 4.2. This input to the A.D.C. is buffered by differential pair Q813 and Q814, the gain of which is defined by R901 and preset R900. The output of this pair is bandwidth limited to 10MHz by R902 and C877, the high frequency common mode is removed by C804 and C805. Resistors R903 and R911 feed the signal to a second differential pair Q815 and Q816, which form part of a shunt feedback amplifier. The junction of R911 and R907 is the relative earth and R918 is the feedback, gain defining resistor. Shift is introduced at this point via R912.

Digital and Analogue shifts are matched by Op. amp U840b with the gain and offset controls. The differential shift input is fed through R885 and R890 and attenuated by R888 and preset R889, the gain adjustment. The resulting signal is applied to the differential inputs of U840B, a variable offset is introduced here by preset R892. The gain of the op. amp. is set by R887, with C874 making the circuit into a simple low pass filter. The output is decoupled by C900 before being added to the Y signal by R912.

The composite signal, Y plus shift, is buffered by Q817 which also provides an inverted signal to drive the 'blow-by' capacitor, C886. The emitter of Q817 drives a second, emitter follower, Q818 through a zener diode D805. This provides a voltage drop which defines the operating point of the collector of Q816. Q818 is loaded by the sample gate, D814 to D817 and a constant current load formed by Q819, with compensation diode D819.

The sample gate is formed from six schottky diodes D813 to D818. D813 and D818 clamp the reverse biasing pulse to 0.4V and −2.5V respectively. This holds diodes D814 to D817 reverse biased with respect to the input signal, and so provide a high impedance to the sample capacitors C889 and C890. When the gate is open D813 and D818 are reverse biased and D814 and D817 are forward biased. In this manner D814 to D817 provide a low impedance path from the A/D amplifier to the sample capacitors. After an initial settling time the voltage on C889 and C890 reaches that of the amplifier. When the gate is closed this voltage is stored until the gate is re-opened. For each sample the gate is open for 10nS, one such sample is taken every 50nS irrespective of the timebase range. In the closed state a small amount of the signal is coupled through the gate by the diode capacitance. This unwanted portion of the signal can be removed by the blow-by capacitor C866, which adds an equal amount of inverse signal.

The voltage stored on the sample capacitor is buffered by U845, a dual F.E.T. This is arranged as a source follower and current source in a single package. In this configuration close offset and thermal matching is obtained, ensuring a low offset between U845 gate and the base of Q820. The emitter followers Q820 and Q822 provide a low output impedance to drive the A.D.C. U842. Transistor Q821 limits the output voltage to 0.25V, this is achieved by clamping the emitter of Q820 to 0.95V.

The A/D converts require input signals between OV and the level set by the negative reference. This reference voltage is generated by zener diode D820 and potential divider R942 and R941, to give −2V. This is buffered by op. amp. U841A and emitter follower Q823. Each A.D.C. is decoupled at its reference input by an indicator and a tantalum capacitor, L814 and C866 for CH1.

The A.D.C. U842, performs its 8 bit conversion in two halves, fir the 4 M.S.B.s are converted as the rising edge of CK, then the 4 L.S.B.s on the falling edge of CK. This requires that the input signal is a constant voltage for a period not less than the high cycle of CK. The outputs of the A.D.C. are E.C.L. compatible and require conversion to T.T.L. before storage, see section 4.8.

The 20MHz clock used by the A/D is generated in the digital timebase circuit, see section 4.10. It is sent differentially over a transmission line to line receiver U846B. The inverted output of U846B is used to drive the A.D.C. via U847c and U846a. The sample gate drive requires a differential input, one side of this is delayed by 10ns by L807, C909, L806 and C908. This produces a 10ns wide pulse at the output of U847a for each rising edge of the clock. Differential pair Q824 and Q825 amplify this to give a swing of 2.5V at the collectors. Each transistor drives are winding on T802, the third winding is capacitively coupled to the sample gate by C887 and C888. The sample gate is opened during the 10ns pulse as previously described.

Fig. 8 shows a timing diagram for the A/D converters.

4.10 DIGITAL TIMEBASE CIRCUITRY

This circuit is shown in Fig. 26.

The timebase setting is encoded into 8 lines, 7 from the timebase switch and one from the s/ms button. These are read by the microprocessor through U832 and are buffered by U831 before going to the F.P.L.A., U828. A data selector is formed by U831 and U833, the signal TBI selecting the required output. When Low U831 is selected and the timebase speed is set by the front panel controls. When high U833 is selected giving the microprocessor control of the timebase setting, see section 4.17 . The F.P.L.A. encodes these 8 outputs into 5 lines for the U.L.A. and indicates underrange and overrange settings. For ext. clock and at higher timebase ranges, 0.2ms/div and above, the F.P.L.A. forces the U.L.A. into Refreshed mode.

A table of inputs and outputs for the F.P.L.A. is shown in the fault finding section 5.3.

For timebase ranges of 0.5ms/Div or slower the U.L.A. generates the required acquisition clock. At higher ranges the clock is generated by repeated divisions of the master system clock. The master oscillator for the oscilloscope is formed by the 40MHz crystal oscillator module XL801, and transistor Q827. The base of Q827 is driven high during realtime operation, disabling the module. The 40MHz signal is divided by two in U835a to give a 20MHz clock with 50% duty cycle. The 10MHz and 2MHz clocks are generated in U820a by division of 2 and 10 respectively. The 10MHz clock is divided by 2 in U821b to give 5MHz, which is further divided by 5 and 10 to give the 1MHz and 500 kz clocks. A nine input data selector is formed by U823 and U909a, the output of which gives the required clock for the selected timebase range.

Control signals A, B and C are generated by U828 and U827, slave is an external signal allowing a user clock to be selected. The select line of U827 is driven by U909b, which forces it low for external clock and follows RSS when ECE is high. When low the U.L.A. clock code is on A, B and C. When high A, B and C are connected to three lines of the timebase switch which code for the 5μs/Div to 0.2ms/Div settings. The output enable of U827 is controlled by transfer clock enable, during acquisitions this is low, allowing the correct timebase code to be selected. When high the outputs of U827 are pulled high by N816, which gives the code for the transfer clock.

RANGE	A	B	C	slave	CLOCK
5μs/Div	1	0	0	0	20MHz
10μs/Div	1	1	0	0	10MHz
20μs/Div	1	0	1	0	5MHz
50μs/Div	0	0	0	0	2MHz
0.1ms/Div	0	1	0	0	1MHz
0.2ms/Div	0	0	1	0	500kHz
–	0	1	1	0	ULA Time Base
–	0	1	1	1	EXT. CLOCK
–	1	1	1	X	200kHz Transfer CLK

The 20MHz clock for the A/D is taken from U835a and converted to E.C.L. by U834. U826a drives the transmission line which connects it to the A/D circuit, see section 4.9.

4.11 FAST STORE CONTROL CIRCUITRY

This circuit is shown in Fig. 25.

All timing in the store control circuit is related to the acquisition clock, the generation of this is described in Section 4.10. The clock is converted to E.C.L. by U834 and synchronised to the 20MHz clock by U824a. When 20MHz is selected as timebase clock it bypasses U824a, going through U825b. The code for 20MHz is detected by U829a; U829b and U883a. The output of U883a is converted to E.C.L. by U834, when high it forces U824a into reset and selects the 20MHz clock via U825b. The resulting clock is synchronised to the start and end of acquisitions by U824a and U825c. Clocking ceases immediately after the following edge of 'count inhibit', but begins on the second clock after the rising edge. 'Count inhibit' is used to gate both acquisition and transfer clocks.

During acquisitions the output of U825c drives the store address counter and generates the write enable, $\overline{WE}$,pulses U819a and U819b delay the rising edge of the clock by 10ns, which extends the low cycle of the $\overline{WE}$ pulses. This ensures a minimum write period of 35ns, when the 20MHz clock is selected. $\overline{WE}$ pulses are inhibited during transfer by 'write clock enable'. The store address is generated by a 10 bit synchronous counter formed from U816, U817 and U818. This counter has no set starting point, it continually cycles round while 'count inhibit' is low. The number of counts per acquisition is not necessarily 1024, as the number depends upon the trigger input and the pretrigger setting, see section 4.12.

4.12 PRETRIGGER CONTROL CIRCUIT

The function of the pretrigger control circuitry is:

(a) To ensure that enough data has been acquired by the fast store to satisfy the pretrigger requirements, and at that point to accept the next trigger.

(b) When the required amount of posttrigger data has been written into the fast store, this circuitry then ends the acquisition phase, preventing further data being written into the fast store.

(c) When an acquisition has been completed, this circuitry then initiates a transfer sequence during which data is transferred from the fast acquisition store into the slower display store. At the end of this sequence another acquisition phase is initiated if the CONTINUOUS CAPTURE mode is selected. Otherwise no further activity occurs unless another acquisition is initiated manually.

The circuit elements involved with pretrigger control are U851d, U870a,b, U882d,e,f, U884, U885, U887a, U889, U890, U891, U892, U893, U894, U895, U896, U897, U898.

The centre of the control circuitry is the ten bit pretrigger counter consisting of U891, U892, U893 and U898c. U891a is a J–K bistable arranged such that its output state changes at each +ve transition on the clock input. U891b is the other half of this dual bistable but is arranged so that its output changes state only if the Q output of U891a is high, on the next +ve clock edge. Hence these two bistables form a two bit binary counter, their Q outputs following the sequence 00, 01, 10, 11, 00 etc. each change occurring on a +ve clock edge. U898c detects the state 11, producing a high signal on its output, enabling the four bit binary counter U892 to increment by one, on the next +ve clock. When U892 reaches maximum count the trickle carry output goes high for one clock, and since U898c pin 10 is high, U893 is enabled to increment by one. The Qc output of U893 will therefore go high after a total of 256 clocks, the Qd output after 512 clocks, and the trickle carry (TC) after 1023 clocks.

An acquisition is initiated by one of three signals, each being a negative-going pulse 100μs long.

1. A signal produced by the monostable. U868a, whose length is set by N810a and C946. The monostable will fire when the B input is high, and this occurs if U909c output is high. Normally the selector U909 is set so that the "A" inputs are selected. (The "B" inputs are only selected if the instrument is in the "SLAVE" mode, see section 4.18). Therefore U868a will only fire if the ARM signal from the Function Switch OCB is low, or the microprocessor ARM signal is low. (see section 4.17).
2. A signal produced by the monostable U868b, whose length is set by N810b and C947. U868b will fire if the RELEASE signal from the Function Switch PCB is low, or the microprocessor RELEASE signal is low (see section 4.17).
3. A signal produced by U885b, a monostable, whose length is set by N810d and C949. This monostable will fire at the end of the transfer phase if the instrument is in CONTINUOUS CAPTURE mode. This mode is indicated by a high at the output of

latch U867b, which is set by RELEASE signal, and cleared by the ARM signal.

If one of these three negative going signals occur the output of U870a will be taken high for the duration of that signal, taking low the output of U851d. This will apply a reset signal to U894a,b and the pretrigger counter described earlier in this section. Resetting U894 takes U896b pin 7 low, enabling the write counter which controls the fast store address lines. (see section 4.11).

The low output of U896b pin 7 is clocked through U884a at the next transfer clock, taking low the Q output, which is the TRANSFER CLOCK ENABLE. (see section 4.11). The fast store can now begin acquiring data.

The circuit behaviour now depends on the PRETRIGGER amount selected, which is determined by the PER25 and PER75 signals. When the instrument is in LOCAL (see section 4.17) these are provided by the Function Switch PCB (see section 4.6). When in REMOTE (see section 4.17) they are set by the microprocessor through U904 pins 12 and 15.

0% PRETRIGGER

PER25 and PER75 are both low, taking low both pin 4 and pin 1 of U897. Since the counter has been reset, pins 2 and 5 of U897 are also low, taking high the output of U898d. U890d pin 11 is also high unless PER25 and 75 are both high, thus selecting the "B" inputs of selector U896, and so taking high U890b pin 4. U894b was reset initially, and so U890b takes low the D input of U895b. On the next negative transition of the write clock (See section 4.10) the Q output of U895b will follow the D input, forcing high U889b pin 6. U884a pin 6 is low (see above), taking high U870b pin 6. Hence the output of U889a is low, preventing both write clocks and transfer clocks from clocking the pretrigger counter.

When a trigger pulse is produced either by the trigger circuit (section 4.3) or the free run circuit, (section 4.3) a high is clocked from U894b pin 12 to U894b pin 9, taking low U894b pin 8, and taking high U890b pin 6. On the next negative write clock edge the Q output of U895b pin 9 is taken high, enabling the write clock to pass through U889b,a so that the pretrigger counter will begin counting from the all zeros state at the write rate. When the counter reaches a count of 1023 the TC output of U893 will be taken high. On the next write clock the Q output of U894a will be taken high, and the counter will again reach an all zeros state. Since U894a pin 5 is now high, U896 pin 7 will be high and U889b pin 3 will be low gating off the write clock to the counter.

25% PRETRIGGER

PER 25 is high and PER 75 is low, taking high U897b pin 4 and U896 pin 1, (which selects the "B" inputs of U896) and taking low U897a pin 1. Since the pretrigger counter is reset U897a pin 2 and U987b pin 5 are both low taking low U898d pin 13, and U896a pin 4, forcing high U890b pin 6. On the next negative write clock edge the Q output of U895b is taken high, taking low U889b pin 5. Since U894a is reset U889b pin 3 is high enabling the write clock to clock the pretrigger counter which will increment from the all zeros state at the write clock rate. When the counter reaches a count of 256,U893 pin 12 is taken high, taking high U897b pin 5 and hence U898d pin 13. This results in U890d pin 4 and the D input of U894b being taken high. U894a is reset still and so U890b pin 6 is high. Therefore at the next write clock pin 9 of U895b will go low forcing high U889b pin 6, and disabling the write clock to the counter. At the same time since U894b pin 12 is high when the next trigger or free run signal occurs and clocks U894b it will take high pin 9 and low pin 8, and via U890b force high U895b pin 12. At the next write clock negative edge U895b pin 9 is taken high again re-enabling the write clock to the counter which will begin counting on from the count at which it was stopped. As described above when the counter reaches a count of 1023 the TC output will go high and on the next clock the counter will count to the all zeros state and U894a pin 5 will go high, pin 6 low. The write clocks to the counter are disabled and U896 pin 7 is taken high.

75% PRETRIGGER

PER 25 is low and PER 75 is high, forcing high U897a pin 1, U897b pin 4 and U890d pin 11 (which selects the "B" inputs of U896). The counter is reset and so the output of U898d pin 13, and consequently U896 pin 4, is low, taking high U890b pin 6. At the next negative write clock edge the Q output of U895b is taken high, and since U894a is reset both pin 3 and 5 of U889b are high, enabling the write clock to the pretrigger counter. The counter will increment from the all zeros state at the write clock rate. When the counter reaches a count of 768 both pins 12 and 11 of U893 are taken high, forcing high U898d pin 13 and U896 pin 4. U894 is reset and so both pins 4 and 5 of U890b are now high taking low the D input of U895b. At the next clock to U895b the Q output is taken low disabling the clock to the counter. At the same time since U896 pin 4 is high, when the next trigger or free run signal occurs and clocks U894b the Q output, pin 9, is taken high and pin 8 is taken low. U890b pin 5 is taken low and U890b pin 6 is taken high. On the next negative write clock edge U895b pin 9 is taken high re-enabling the write clock to the counter which will begin counting again. When the counter reaches a count of 1023 the TC output will be taken high. On the next clock the counter will reach a count of zero and at the same time U894a pin 5 is taken high, pin 6 low, disabling further write clocks and taking high U896b pin 7.

100% PRETRIGGER

PER 25 and PER 75 are both high taking low the output of U890d, which takes U896 pin 1 low selecting the "A" inputs of U896a and b. Since U894a is reset pin 5 is low, pin 6 high, forcing low the output of U896a, pin 4, and high the output of U890b, pin 6. On the next

negative write clock edge U895b pin 9 is taken high gating the write clock to the counter, via U889b and U889a. When the counter reaches a count of 1023 the TC output is forced high. On the next write clock the counter will count to zero, and U894a pin 5 is taken high, pin 6 low, disabling the write clock to the counter. U894b pin 12 is now high and when the next trigger or free run signal occurs U894b pin 9 is forced high in turn taking U896b pin 7 high.

Once U896b pin 7 is high the data acquisition phase is completed. This signal directly disables the write enable signal to the Fast store. At the same time U858a pin 3 will be taken high since both inputs are now high, taking high the write counter COUNT INHIBIT signal, holding the write counter at whatever address it has reached. (See section 4.11).

As explained in the Display section, (see section 4.14) when the RWCLK signal is low the address present on the address bus of U910 is the address of the next display data. When this signal is high the address bus provides either the current write address (for the lower timebase rates, see section 4.13) or the transfer address. For timing details see figure 9. When the acquisition is completed i.e. U896 pin 7 is high, the address on the address bus of U910 during the transfer slot is zero, which corresponds to the left hand edge of the display.

U896 pin 7 being high on the negative edge of the next transfer clock U884a pin 6 is taken high, pin 7 low, initiating the following.

(a) U884a pin 6 enables the TRANSFER CLOCK ENABLE signal to the timebase circuitry (see section 4.10), which controls the clocks to the Fast Store write counters.

(b) U884a pin 7 takes low U875c pin 10, taking high U875c pin 8 and U883b pin 6, which enables the NMWE signals to reach the Display Memory and hence data can now be written into the display store at the appropriate time.

(c) U884a pin 6 takes high the B input to the monostable U885a. Since the STORED signal output by U910 pin 3 is low the monostable will produce positive going pulse of 100μs (set by N810c C948) at pin 13 and the inverted version of this pulse at pin 4.

(d) U884a pin 6 takes high the J-K inputs of U884b, and on the next negative edge of the transfer clock U884b pin 10 will be forced high, pin 9 low.

Since U871 pin 13 is high for the RSS mode, the positive pulse from U885a pin 13 produces a positive pulse at U871c pin 8 and U910 pin 47. Following the next transfer clock the transfer address on the address bus of U910 will begin incrementing from zero at the transfer clock rate. (See timing diagram Fig. 11). The negative pulse from U885b pin 4 resets bistable U895a taking high pin 6, low pin 5.

U884b pin 10 being clocked high takes high U870b pin 3, and since U895a is reset, taking high U870b pin 5, the transfer clock appears at U870b pin 6 and clocks the ten bit counter via U889a. At the same time U884b pin 9 is clocked low taking low U858a pin 3, which is the COUNT INHIBIT signal, enabling the write counter to increment. The write counter and the ten bit counter will now be counting together in synchronism with the TRANSFER address on the address bus of U910. During the 1μs period when the transfer clock is high there are two negative going 250ns pulses on the NMWE line, and A10 from U910 is low for the first of these pulses and high for the second. The two 250 ns signals enable the tristate selectors on the Fast Ram PCB and A10 signal determines which channels' data will appear on the output of the selectors. Hence for the first of these pulses Channel 1 data is present on the Display Memory data bus, and Channel 2 data for the second. This data is written into the Display Memory by the NMWE signals at the address contained on the address bus of U910, which is the current transfer address plus the A10 signal. In this manner data is transferred from the Fast Store into the Display Memory at successive addresses. (See Fig. 9 for more details of the timings involved).

When the ten bit counter reaches a count of 1023 the data transfer is completed. U893 TC output will be high and after the next transfer clock the counter will reach zero and U895 pin 5 will be high, pin 6 low. As a result U887a pin 2 is taken high and since U887a pin 1 is also high U887a pin 3 is forced low, resetting U884a and b. U895 pin 6 going low takes U870b pin 5 low disabling the transfer clocks to the pretrigger counter. When U884b is reset pin 10 is taken low. If the CONTINUOUS CAPTURE mode is selected, i.e. U867b pin 9 is high, the monostable U885b will fire producing a negative pulse 100μs long (set by N810d) at pin 12, which takes low U870a pin 12 initiating another acquisition as described earlier.

4.13 DISPLAY MEMORY DATA ACQUISITION

The data written to the display memory can come from one of three sources. At timebase ranges 0.2μs/div to 5μs/div the data is transferred from the FAST Store which has been described in section 4.8. At timebase ranges from 0.5μs/div down to 50s/div the data is written directly from the two latches at the output of the ADC's. In both these cases the circuitry controlling the Display Memory behaves in the same way. The third source is the microprocessor and its method of writing to the display memory is described in section 4.17.

The centre of the circuitry controlling the Display Memory is the Uncommitted Logic Array U910, which drives the address bus of the Memory providing both write addresses for the Data Acquisition/Transfer, and read addresses for the digital reconstruction circuitry (See section 4.14). The master timing signals for U910 are provided by U879 and associated components.

U879 is a four bit decade counter which is clocked by the master 20MHz clock from U835. U880a detects a count of 3 or 7 on the outputs of U879, taking low U881c pin 10. U881b and U881c are arranged as a bistable, therefore taking low U881c pin 10 will take high U881c pin 8. U881a detects a count of 8, taking low U881c pin 8. The output of U881c is high therefore between the counts of 3 and 8, a total time of 250ns. The output of U881a pin 3 is inverted by U882b producing a 50ns pulse on a count of 8. Both the 250ns pulse, which is the WE signal to U910, and the 50ns pulse, which is the MHZCLK signal to U910, occur at a repetition rate of 2Mhz. For further information on the timings of these signals see Fig.8. U910 will provide the following clocks from the two clock inputs.

RWCLK. This is a 200kHz clock of even mark to space ratio, and is used to indicate when a write or read address is output to the Display Memory. When the clock is high a write address is present on the address bus, and when low a read address is present on the bus.

EWRITE is a 1μs pulse which occurs at a repetition rate determined by the timebase code on the D1, D2, DIV2, DIV5 and DIV1K. This signal is only used when the Fast Store is being used, at timebase ranges 0.2ms/div to 5μs/div. In this mode EWRITE has a repetition rate of 200kHz.

TBOUT. This signal is a clock whose rate indicates the acquisition rate, except on the ranges when the Fast Store is active, when it is 200Khz.

In addition to these clocks U910 provides the address bus for the Display Memory and the Not Memory Write Enable signal, NMWE, which controls the WE signal of the Display Memory. Further timing information is given in Fig. 10.

In this section we are concerned with only the data acquisition into the Display Memory. This occurs in one of three modes.

(a) Repetitive Single Shot (RSS). This is the mode when the data from the ADC's is written into the Fast Store initially, and then transferred into the Display store. This mode of data transfer is described in section 4.12.

(b) REFRESH. In this mode data is transferred into the Display Store beginning at location 0 in the memory for each channel, the data being transferred from the direct from the ADC latches. The data storage process is initiated by an NARM signal at U910 pin 63 or internally in U910 by the end of the previous acquisition. U910 sets the write address to 0 and holds it until a trigger signal is input into the TRIG input of U910 pin 47. The write address will now increment at the acquisition rate selected by the Time/div switch. The data is latched into the ADC latches by the EWRITE signal. While EWRITE is high there will be one or two negative pulses on NMWE of 250ns duration. These pulses enable the data selectors on the Fast Store PCB routing data from the ADC latches to the Display Store data bus. The CH2 signal produced at U910 pin 28, which is low for the first pulse of NMWE, and high for the second, controls the data selectors ensuring that CH1 data is presented to the Display Store during the first NMWE pulse, and that CH2 data is presented during the second pulse. When the NMWE pulse, and that CH2 data is presented during the second pulse. When the NMWE is taken high the Display Store latches the data present on the data bus into the address selected by the address bus.

If the instrument is in either CH1 or CH2 mode only NMWE will only go low once, ensuring that the channel not selected is not updated. The NMWE signal to the Display Store is modified by the HOLD or LOCK DATA signals. If the HOLD DISPLAY control is operated NMWE is taken high via U883b, U880b and U858d, and the write address to the Display Store is held, preventing the Display from changing. If either of the LOCK DATA controls is operated the NME signal for the relevant channel is gated high via U887c, U887d, U880b and U858d, the write address being unaffected. The data in the Display Store is then locked for the Channel selected.

When the write address reaches 1023 the acquisition is complete. If the instrument is in SINGLE SHOT CAPTURE mode the STORED signal from U910 pin 3 will be taken high, which switches on the STORED l.e.d on the FUNCTION SWITCH PCB via U878e, and takes low U886 pin 12 which resets U867d, switching off the ARMED l.e.d. If the instrument is in the CONTINUOUS CAPTURE mode the next acquisition will begin.

(c) ROLL. Data acquisition is the same as the REFRESH mode except that the write address behaves differently.

If SINGLE SHOT CAPTURE mode is selected the write address will begin incrementing immediately at the required acquisition rate. New data will be written into each address in the same way as described in (b) above. When U910 has ensured that enough data is contained in the Display Store it will accept the next TRIG signal, and when the required amount of post trigger data is in the Display Store the acquisition will be ended, and the write address will be held. The STORED signal will be taken high and as described in (b) will light the STORED l.e.d and clear the ARMED l.e.d. The acquisition is then complete.

If the instrument is in the CONTINUOUS CAPTURE mode the write address will increment at the acquisition rate, but will cycle from 0 to 1023 continuously, writing data into each address in turn.

Triggers are ignored and the instrument captures data continuously.

The LOCK DATA and HOLD DISPLAY controls behave as described in (b) above.

4.14 DIGITAL Y RECONSTRUCTION

As explained in the previous section 4.13 the ULA U910 outputs a read address when RWCLK is low. The data contained in the Display Store at this address is latched by U862 which is clocked by the +ve edge of the RWCLK signal via U888b and U881d. The read address is synchronised to the digital ramp output on the DAC pins of U910 (see next section). In the modes when the ROLL signal to the ULA is low the read address is the same as the DAC address. This ensures that the data at location zero in the Display Store for either CH1 or CH2 is positioned at the left hand edge of the display. If the mode selected is such that the ROLL signal to the ULA U910 is high there is no correspondence between the read address and the DAC address. This is necessary to produce the ROLLing effect. The difference between the read address and the DAC address is increased everytime there is a byte of data written into the Display Store producing an offset between the display data and the display X ramp which increases at the write rate. The timing is shown in Fig. 9. The two channels are read out alternately, one channel per sweep of the digital ramp generator, unless single channel mode is selected.

The Y data present on the output of the latch U862 is converted into an analogue form by U861, a monolithic 8 bit digital to analogue converter. A reference current of 1mA is fed into this device and the outputs Io and $\overline{Io}$ produce a differential current proportional to the product of the reference current and the digital code present on the data inputs D0 to D7. Note that D7 is the 1sb of this device. The reference current is derived from a 6V2 voltage reference formed by zener diode D834, and R1022 decoupled by C918. The reference current of 1mA is defined R1020 and R1021, producing a range for Io and $\overline{Io}$ of 0 to 1mA depending on the data input. Approximately on quarter of the current outputs are fed into the differential amplifiers U860a and U860d which convert the currents into a voltage output of 280mV approx.A time constant of 1μs, set by C924, R1004 and R1005, is applied to this differential output, which matches the time constant of the digital ramp generator. This produces a dot joining effect, the dot moving linearly between the data points. However the brightness is not linear between dots. An adjustment of the relative d.c. offset between the two differential Y output signals is provided by R1009, and R1006 provides a gain adjustment. The output of the differential amplifier is fed via R1000 and R1001 into the beamswitch described in section 4.2.

4.15 DIGITAL RAMP GENERATION

The ULA U910 provides a linearly incrementing address bus DAC1 to DAC10 to drive a ten bit digital to analogue converter U863. The lines DAC1 to DAC10 increment from 0 to 1023 as the Y data is read out from the store, 0 corresponding to the left edge of the screen. These ten lines drive U863 which produces the differential current outputs Io and $\overline{Io}$. These outputs represent the product of the reference current into the device and the data present on the data inputs. The reference current of 1mA is set by R1025 and R1026 which are connected to the 6V2 voltage reference, mentioned in 4.14, and 0V. The current output Io is fed to U864a which converts it to a voltage output. The gain of this amplifier is set by R995 and the d.c. level of the output is set by R992. A time constant of 1μs is produced on the output by C935, R982 and R996 to match the Y output time constant. The output of the DAC has a glitch at the changeover of the m.s.b. so to reduce this a portion of the m.s.b. is fed into the non-inverting input of U864a to compensate for the glitch. The output of U864a drives one input of the multiplexer U859a, and in the storage modes is directed to the X output amplifier.

U910 pin 52 produces a blanking signal for the duration of the first four data points on the display i.e. 20μs long. This blanking signal is multiplexed with the analogue blanking signal by U877. In the storage modes the digital blanking drives the amplifier formed by Q832 which adjusts the level of the pulse to match that required by the blanking amplifier described in 4.19.

4.16 CURSOR SWITCH PCB

This circuit is shown in Fig. 19.

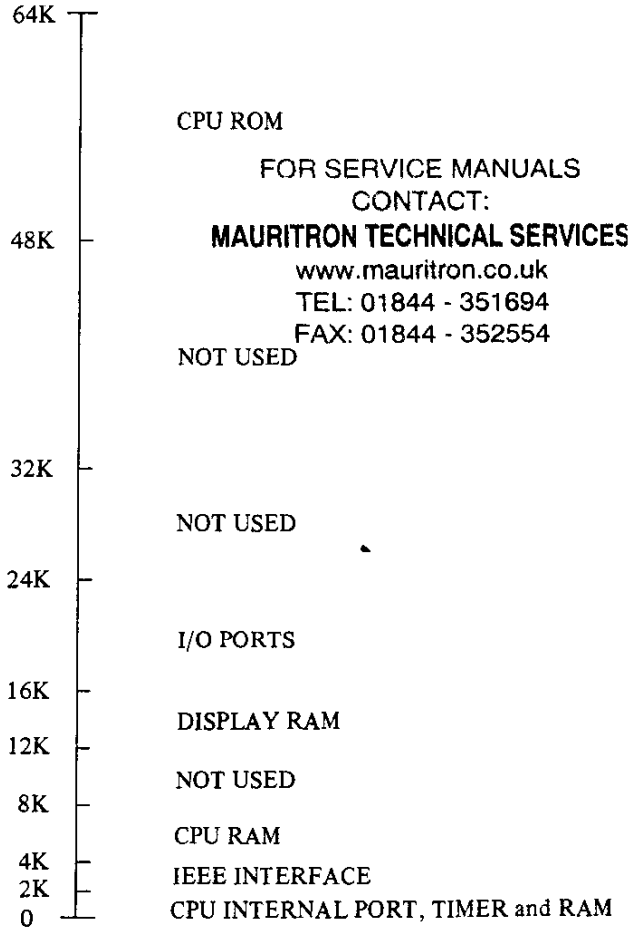
The instrument power on indication is provided by D1901 with R1901 limiting the current through the diode. The REMOTE l.e.d. is turned on by Q1901 which is driven by the LOCAL line, see section 4.17. When LOCAL is low the l.e.d. is ON. Switches S1901 to S1905 are the cursor control buttons. When pushed each switch connects its control line to ground, pulling low one of the inputs to the microprocessor I/O port. Pull ups are situated on the CPU board.

4.17 CPU BOARD

The CPU Board is based around the 6303, a 1MHz CMOS microprocessor. A block diagram of the board is shown in Fig. 3.

A breakdown of the memory usage is shown below.

The circuit diagram for the CPU Board is shown in Fig. 20.



POWER ON RESET

When the 6303 microprocessor powers up it must be forced into its required mode of operation, in this case the multiplexed mode. This is achieved by holding U1501 pins 8 and 9 at 0V, pin 10 at +5V while pin 6 is held low for approximately 100ms and then brought high. A slow ramp is produced by C1506 and R1501 which drives U1501 pin 6 and the select lines of U1504. The threshold of U1501 pin 6 is set lower than that of U1504 so the reset is completed before U1504 changes the inputs.

MEMORY DECODING

This is performed by U1520, U1521, U1522, U1537b, c and U1534c.

The memory is divided into 16K sections by U1522a. The section from 16K to 32K is divided in half by U1537c which gates the output with A_{13}. This output is broken down into 2K blocks by U1520 and U1521. These two I.C.'s are enabled by the R/W line from the microprocessor on such a way that U1521 decodes the write only ports and U1520 decodes the read only ports.

The lowest 16K portion of memory is broken down into 4K blocks. The lowest 4K of which is divided in half by U1534c and U1537b. This leaves the lowest 2K of the memory map undecoded, the ports appearing in this area are internally decoded by the microprocessor.

ROM and RAM

The CPU board has 16K of programme ROM, U1507 and 2K of RAM, U1523.

PLOT

The CPO has two plot modes GPIB and analog plot. The GPIB plot is controlled by software and outputs through the IEEE interface.

The analog plot is a simultaneous output at both channels and is provided by U1526, U1529 and associated components.

The Digital to Analog Conversion is performed by U1526 a dual monolithic current output DAC. These outputs are converted to voltages by U1529a and U1529c for CH1 and CH2 respectively. They are then scaled by two op-amps U1529b and U1529d to give a full scale swing of 800mV. Resistors R1517 and R1522 introduce an offset to give outputs in the range -0.4V to +0.4V. A simple low pass filter is provided by R1518, C1518, R1519 and C1519.

DSO INTERFACE

This circuit is formed by U1514, U1515, U1516, U1517, U1518, U1519, U1531, U1532, U1533 a,b,f, U1534 a,b,f, U1535 a,c, U1536, U1537d, U1539, U1546 and U1547.

The DSO Interface provides access to the DISPLAY RAM and all of the I/O ports situated on the DSO board.

When the I/O ports are addressed U1546 pin 1 is set high, this connects the B inputs of U1546 to y outputs. U1518 and U1519 are now held in their transparent state. When a read port is addressed U1547b goes low enabling the output of U1519. This creates a path from the input port through U1519 to the microprocessor. When a write port is addressed U1537d goes low enabling the output of U1518. This creates a path from the microprocessor through U1518 to the output port.

If the instrument has at any time since power up been in ROLL mode then the left hand edge of the CRT display has no set address within the DISPLAY RAM, see sections 4.12 and 4.13. For the microprocessor to access the DISPLAY RAM it is necessary for it to know how the left hand edge of the screen relates to the DISPLAY RAM address.

The signal $\overline{RTC}$ is a 5μs pulse which goes low when the right hand edge of the display is reached. This is used by U1516 and U1517 to capture the display address at this point. The terminal count address is then used by the microprocessor to calculate physical addresses within the DISPLAY RAM.

When the DISPLAY RAM is addressed U1536 pin 1 is set low, connecting the A inputs of U1546 to the Y

outputs. If the operation is to be a write then U1531 pin 9 is also set low. Data is then written to the correct DISPLAY RAM address. If the operation is a read dummy data needs to be written, it is still necessary to set up the DISPLAY RAM address. The data is stored in U1518 and the lowest 11 Address lines are held in U1514 and U1515. The microprocessor sets U1531 pin 6 high clearing the reset on U1532. This enables $\overline{\text{RWCLK}}$ to be shifted through U1532 at a rate of 0.5μs a bit. The gating around U1532 combines these shifted outputs to give the signals detailed in the timing Diagram Fig. 16. The T/W signal, U1547 pin 8 only goes low during write cycles. If the operation was a read then the data is stored in U1519, which the microprocessor can get by reading any valid DISPLAY RAM address.

IEEE INTERFACE

The circuit elements involved are U1510, U1511,U1512, U1513 and S1501.

The IEEE bus is brought from the back panel to the CPU board by SKCC. This is buffered by U1512 and U1513 before entering the bus controller U1511. All the necessary bus protocol is handled by this I.C. The address switch can be read by the microprocessor by addressing it through U1511 which enables the output of U1510.

ALPHANUMERICS AND CURSOR GENERATION

The circuit elements involved are U1530, U1531, U1533c, U1535d, U1541, U1542, U1543, U1544 and U1545.

An internal functional diagram of the PAL, U1538 is shown in Fig. 18. A timing diagram of its function is shown in Fig. 15.

Every 15ms the PAL initiates an alpha cycle, this is done by stealing one of the ULA display cycles. Exactly 5ms is allowed for the display of the alphanumerics before the PAL relinquishes control to the ULA.

At the beginning of an alpha cycle NMI is taken low causing an interrupt request in the microprocessor. The display dot is positioned one quarter of the way across the screen in X and just above the base line in Y. This drives the output of U1535d high enabling U1542 and U1543 to count. When 192 is reached U1535d goes low again disabling further counting. These outputs form the 8 most significant bits of the X DAC and cause a half screen line to be drawn. The alpha ram, U154[illegible], is also addressed by these 8 lines and its output forms the blanking signal which is superimposed onto this line. The microprocessor detects when U1535d goes low and then draws another line in the same manner but slightly lower. Seven lines in total are drawn, giving 16 characters on a 7 x 8 grid.

At the end of the seventh line U1531 pin 5 goes low which disables the clock to U1542 and U1543. These now behave like latches. The microprocessor draws the cursor as a series of dots by directly controlling the X and Y DACS. X data is placed on the address bus, (10 bits) and Y data on the data bus (8 bits). The X DAC latch is formed by U1541, U1542 and U1543 with the buffer formed by U1530 and U1540. The Y DAC latch, U911, is situated on the DSO board.

I/O PORTS

Throughout the DSO and CPU boards there are 9 input ports and 7 output ports. The tables show in detail which control lines are present at each port.

The LOCAL and TBI lines control the LOCAL/REMOTE status of the instrument. TBI controls only the timebase settings where as LOCAL controls all other digital functions. When LOCAL is high U899 is selected, when low U904 is selected giving the microprocessor control at the instrument.

4.18 EXTERNAL CONTROL CIRCUITRY

These circuits are shown in Figs. 16,17.

All signals and control lines for the external control circuitry are available from the 15 way D type connector on the back panel. These connections are detailed below.

EXTERNAL ARM/ARM ENABLE

EXTERNAL Arm is positive edge triggered and Ext. Arm enable is active high.

When external arm is selected, the D input of U866b is driven low and the rising edge of the external arm clocks it through to the Q output. This is routed through data selector U838a to the arm control circuitry and the falling edge causes an arm U866b to reset by 'stored', when the ULA receives the arm. If Autoplot is selected the D input of U866a is held high, inhibiting arms, until plotting is complete.

$\overline{\text{ACQ GATE}}$

$\overline{\text{ACQ}}$ gate is an active low signal indicating that the instrument is in the process of acquiring a trace.

MASTER ARM IN/OUT

Master arm is an alternative method of arming the instrument. When selected all other arms, push button, AUTOPLOT and EXT Arm, are ignored. MASTER arm is selected when slave enable is high.

Master arm out is a copy of the current arm signal seen by the instrument. In the case where slave enable is active it copies Master arm in.

EXT CLOCK IN/OUT

EXT clock out is a copy of the acquisition clock and if slave enable is active it will follow EXT clock in. In slave enable or for timebase ranges of 0.2ms/Div or faster external clock out consists of a burst of acquisition clock (with $\overline{\text{ACQ GATE}}$ low) followed by a 200KHz clock (with $\overline{\text{ACQ GATE}}$ high).

EXT clock in is selected by slave enable and when active it is taken as the acquisition clock. It is synchronised to the internal 20MHz clock and so it must be less than

Write only ports

								ADDRESS (HEX)
TRIG. EN.	INT	$\overline{\propto}$	$\overline{DACE}$	B	D	BLNK	DUAL	$4800
Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0	$5000
PA_7	PA_6	PA_5	PA_4	PA_3	PA_2	PA_1	PA_0	$5800Y
PB_7	PB_6	PB_5	PB_4	PB_3	PB_2	PB_1	PB_0	$5801
$\overline{REL}$			LOCK	75%	25%	ROLL	$\overline{ARM}$	$6000
S/MS	S_5	S_2	D_0	D_1	D_2	D_3	D_4	$4C00
$\overline{CLR}$	PEN	PLOT LED.	LOCAL	RBI	CH1	CH2		$4000

READ only ports

								ADDRESS (HEX)
ON/ OFF	SET DAT	CH1/ CH2	>	⋘	<	⋙	–	$0002
DIG PLOT	CH1	CH2	LOCK	75%	25%	ROLL	STORE	$4800
EXT ARM	EOL	DR	E	D	C	B	A	$6800
AP1	AP2	H1	H2	RLD	NRM	P1	P2	$5800
–	–	–	–	–	A_{10}	A_9	A_8	$7800
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	$7000
S/MS	D_4	D_3	D_2	D_1	D_0	S_5	S_2	$4400
P_B	P_A	Y_{1F}	Y_{1E}	Y_{1D}	Y_{1C}	Y_{1B}	Y_{1A}	$5C00
X_{10}	P_C	Y_{2F}	Y_{2E}	Y_{2D}	Y_{2C}	Y_{2B}	Y_{2A}	$5000

10MHz, however, there is no lower limit. The display is only updated at the end of each capture, so for slow external clock frequencies it may take an appreciable time between arm and display update.

e.g. For a 1Hz external clock the screen will be updated every 17 minutes.

SLAVE ENABLE

When slave enable is high master arm in and EXT CLOCK in are selected. In this way it is possible to connect two or more instruments together and control them from one.

MASTER		SLAVE
Ext clock OUT	→	Ext clock IN
MASTER ARM OUT	→	MASTER ARM IN
$\overline{\text{ACQ}}$ gate	→	Ext TRIGGER
slave enable to Ground		slave enable to +5V

By selecting −ve trigger slope on the slave both instruments will capture simultaneously, giving four traces. With +ve trigger slope the slave will capture after the master has completed its acquisition, give two double length traces. This second method will only work for timebase ranges of 0.5ms/cm or slower.

4.19 POWER SUPPLIES AND C.R.T. CIRCUITS

Circuits for the power supplies are shown in Fig. 28, 29.

The following D.C. supplies are generated in the power supply circuits from secondary windings on the supply transformer T1.

+210V, +17V, +11V, +7V, +5V, −5V, −11V, −1850V.

The +17V, +11V, +5V, −5V and −11V supplies are generated on the Auxillary power supply board. The +210V, +7V and −1850V supplies are generated on the main analogue board.

The +5V and −5V supplies are derived from a single 8V−8−8V, center topped winding of transformer T1. The output is rectified by the diode bridge U1301, into smoothing capacitors C1301, C1302 and C1303 for +5V, and C1304 and C1305 for −5V. The outputs are stabilised by series regulators U1302 and U1303, and decoupled by C1306 and C1307 for +5V and −5V respectively.

The three supplies +17V, +11V and −11V are derived from a single 13V−0−13V, center topped winding on T1. A mains trigger pickoff is taken from this winding via R1309 and C1317, which form a low pass filter. The output of the winding is rectified by the diode bridge formed from D1303, D1304, D1305 and D1306. The negative side of the output is smoothed by capacitors C1311 and C1312. The positive side is smoothed by C1309 and C1310, the +17V unregulated is taken from this point. The stabilised +11V supply is formed from the +17V by the series regulator U1304 and decoupled by C1313. The −11V is generated in a similar manner by U1305 and C1314.

The output from the 210V secondary is bridge rectified by the four bridge-connected diodes, D722 to D725, into the reservoir capacitor, C705. The resultant d.c. voltage protected by FS701 feeds the h.t. regulator for the +210V supply. D730 is the reference for this supply, buffered by emitter follower, TR711, and the Darlington pair, TR713. The return of the rectified 210V supply is via the 11V line to balance load currents in the low voltage supplies.

The +7V supply is provided from the +11V supply by a further 12V series regulator, IC701, operating with respect to the −5V line.

The grid and cathode supplies for the c.r.t. are derived via the voltage doubler circuit D718, D719, C711 and C712, from the 950V secondary of T1. The negative side of the unstabilised supply developed across C711 and C712 is held at approx. −200V with respect of 0V by the series zener diode, D706, which is returned to the stabilised cathode potential of −1850V. Subsequent variations in the unstabilised supply are developed across the series regulator, TR707, of the e.h.t. regulator. The feedback path of this regulator uses the current from the −1850V line defined by the resistors R715, R714 in parallel with R744 (the Focus pot.) and RN720e. The latter being within the e.h.t. network. This current is returned to the +7V line via R731, R725 and R726. If the resultant potential of the tap point defined by the preset, R725, is not at approx. −4.5V, the current in transistor, TR706 will change to correct the stabilising voltage across TR707, TR706 and TR707 are connected in cascode.

The heater of the c.r.t. is supplied directly from an independent 6.3V secondary winding of T1.

The 4030 employs a novel modulation circuit to control the grid potential with respect to the cathode potential. The transistor pair, TR703 and TR704, generate an essentially constant current from the collector of TR703. This generates a constant voltage across RN720 and preset, R713, and is returned to ground via the output of the bright-up amplifier. Thus signal variations from this amplifier which operates with respect to 0V are transferred with the large negative d.c. offset to the collector of TR703, to be applied to the grid of the c.r.t. via the emitter follower, TR716.

In more detail, the constant current from TR703 is defined by the emitter resistance, RN720c and the base potential, from the divider, RN720a and RN720b.

This constant current source is returned to the −200V line (negative of D706) so that the collector of TR703 (the c.r.t. grid) can move negative from the cathode. The collector potential is protected by D705 against excessive swing during switch-on or switch-off conditions. While

RN720d and R713 generate the necessary large d.c. potential to couple the bright-up signals to the grid, the high frequency components are by-passed through C702.

The bright-up signal amplifier is formed by the cascode transistor pair, TR701 and TR702, with shunt feedback via R704. It responds to the sum of three inputs. The first is a d.c. bias via R707 from the INTENSITY control, R745. The second is the external Z Modulation signal from SKG, via R703. The third is the signal from the blanking selector, U813a, which in NORMAL provides bright-up during each timebase sweep with blanking of each chop transition if appropriate, and in STORE mode provides bright-up on each readout sweep. Diodes, D701 and D702, provide protection against excessive external inputs and with R702, prevent saturation of TR702.

The focus electrode of the c.r.t. is supplies from the focus control potentiometer, R744, with a portion of the −1850V supply. The astig. electrode is supplied from preset, R708 driven from the +210V supply via the divider network R746, R747.

Minor angular misalignment of the gun assembly of the c.r.t. or the effects of externally applied magnetic fields, axial to the c.r.t., can be corrected by the trace rotation coil. This coil is round the neck of the c.r.t. and the current is determined by the TRACE ROTATION control, R737, connected between the ±11V supplies and driving emitter followers, TR714 and TR715.

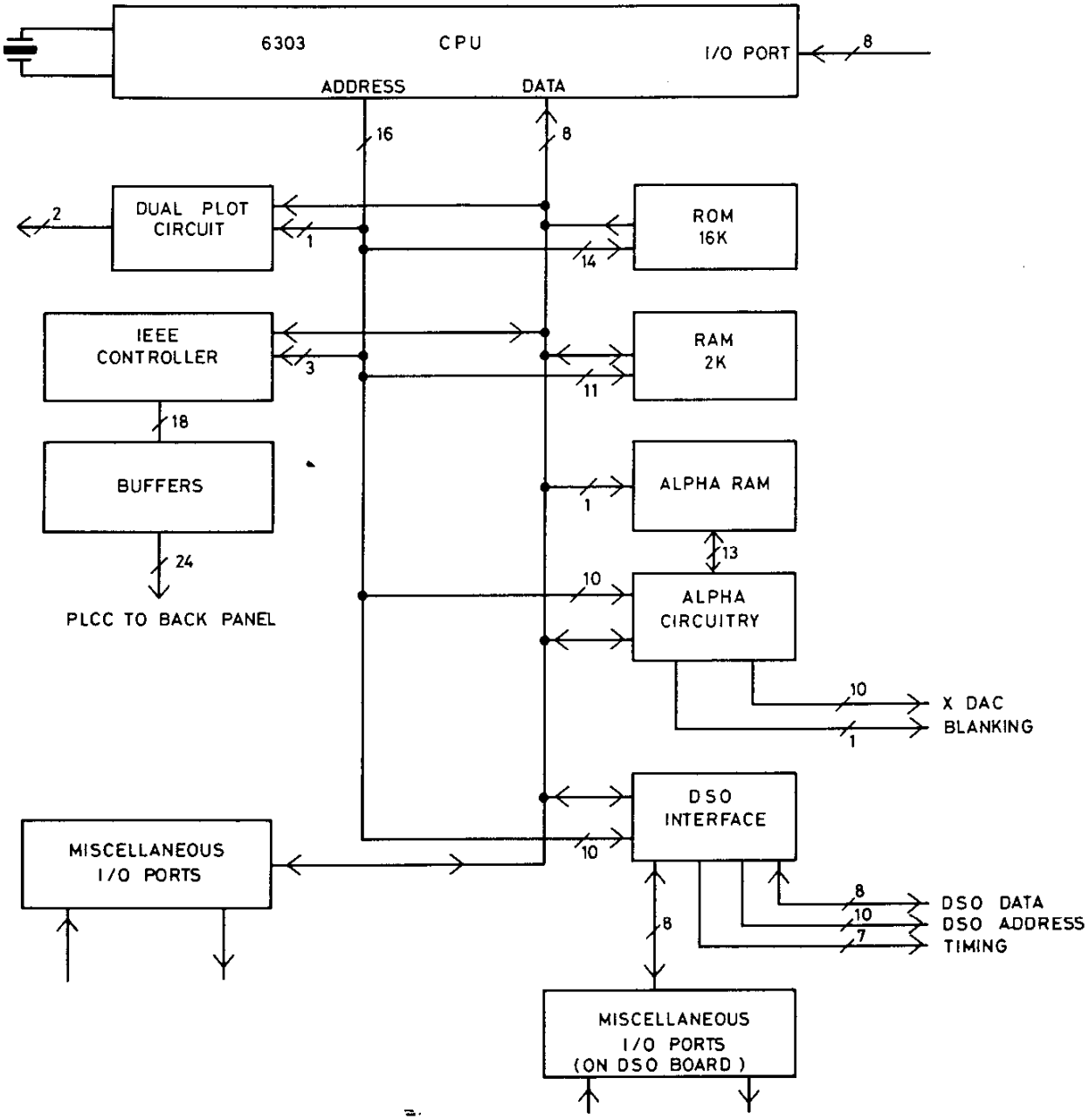


Fig. 3. Block Diagram for 4035 CPU Board

5.1 GENERAL

Figs. 4, 5, 6 & 7 show the internal location of the major components, subassemblies and preset controls. No regular maintenance is required apart from the routine recalibration. The construction of the instrument is such that full access to all the calibration controls and all major components can be obtained once the two halves of the case have been removed.

Supply voltage adjustment is made by the small plug-in pcb on the power connector. This is inserted such that the required supply voltage is visible. The supply fuse is also in the power connector and access can only be obtained by removing the power connector. For 220V or 240V operation a 20mm 1A Slo-blo fuse is required (Pt No.34790) and for 100, 120V operationsa 20mm 2A Slo-blo fuse is required (Pt. No.40569). The intimate H.T. fuse is a 100mA, 20mm fuse.

5.2 REMOVAL OF THE CASE & SUB ASSEMBLIES

WARNING

DANGEROUS VOLTAGES ARE EXPOSED ONCE THE CASE IS REMOVED. MAINTENANCE SHOULD ONLY BE CARRIED OUT BY QUALIFIED PERSONNEL. PARTICULAR CARE SHOULD BE TAKEN ON THE CRT AND THE EHT AREA OF THE ANALOGUE PCB WHERE VOLTAGES IN EXCESS OF 2000V MAY BE RETAINED AS STORED CHARGE FOR UP TO ONE MINUTE AFTER THE SUPPLY IS DISCONNECTED.

(a) To Remove the Case (Top Section)
Unscrew the six fixing screws and lift the cover clear of the instrument.

(b) To Remove the Case (Lower Section)
Turn the instrument over taking care not to scratch the corner castings. Remove the ten fixing screws and lift the cover clear of the instrument.

(c) To Remove the Handle
Using a spanner unscrew the four 100mm nuts retaining the handle to the sidebars.

(d) To Remove the Power Supply Assembly.
Unscrew the four screws retaining the Heatsink Bar to the Rear Panel, and then unscrew the two screws fixing the Power Supply PCB to the C.R.T. Bracket. Remove the connector to the Analogue PCB and the power connector to the D.S.O. PCB. Disconnect the flying cable to the F.I.G. PCB, and cut the Tyrap holding this cable to the F.I.G. PCB shield. The power supply assembly should now be eased away from the rear panel and up from the instrument. The transformer supply connector can now be disconnected from the centre of the PCB.

The assembly should now be free.

(e) To Remove the C.R.T.
Remove the bezel on the Front Panel around the C.R.T. faceplate, exposing four Pan Head screws, which retain the moulding which holds the C.R.T. front. Disconnect the trace rotation coil leads from the Points 734, 735 on the Analogue PCB, and unsolder the two earth leads connected to the C.R.T. shield. Remove the tube base assembly. The base itself is carried on a small printed circuit board which has been designed to allow access to facilitate withdrawal from the C.R.T. pins. Remove the single clamp fixing screw and rotate the two C.R.T. clamp sections by 30° approximately to free the clamp from the C.R.T. bracket. Remove the four screws retaining the C.R.T. front moulding (exposed by removing the C.R.T. Bezel). The C.R.T. can now be slid back from the front panel, the rear of the C.R.T. sliding back through the C.R.T. bracket, with the C.R.T. clamp. The tube can now be lifted up and drawn forward to clear the top edge of the instrument. Remove the clamp, shield and moulding on the faceplate.

To replace the tube follow the instructions in the reverse order, remembering that once the tube is in position, the clamping ring is rotated to hold and lock the tube in place. Also check the polarity of the trace rotation coil reconnections. A clockwise rotation of the front panel should cause a corresponding movement of the trace.

(f) To Remove the Attenuator Assembly.
Should it be necessary during repair to remove the attenuator and screens around the preamplifier for access to components on that board or on the front of the main board, proceed as follows.

Remove the screen covering the preamplifier assembly by unsoldering the three securing points on the screen, and unclipping it.

Remove the collet fitted knob on the timebase switch. Access to the collet securing screw or nut is obtained by prising of the cap on the top of the knob. Remove the small knobs on the rest of the controls, the three knobs on the Internally Focus and Graticule illumination are secured by a collet screw under the cap on the top of the knob, and the rest are pull off types. Unclip the bezel around the C.R.T. by pushing the top of the bezel down and forward. Unscrew the four nuts retaining the front outer panel onto the inner panel. Remove the outer panel, exposing the inner panels. Unsolder and using a desoldering tool clear the solder from the three screens where are earthed onto the preamplifier board.

Unsolder and remove the wires from the CAL 1V pin and the External Trigger connection on the input printed circuit board. Unsolder also the two signal connections to PINS 201 and 231 on the preamplifier board.

The three countersunk screws retaining the small inner panel should be removed. The small panel can now be withdrawn from the instrument. Note the orientation of the switch wafer on the pre-amplifier board with respect to the attenuator switch shaft.

Reassembly is the reversal of the procedures described above.

(g) Removal of the Input Coupling Switch printed circuit assembly.
If it is necessary to gain access to the small printed board which carried the input selection switches and the A.C. coupling capacitors for each Y channel, together with the input network for the External Trigger signal proceed as follows. Unsolder and remove the two wires connecting the input printed board to the attenuator wafer sections of each VOLTS/DIV switch. Desolder the three input B.N.C. sockets from this board and the three screen earthing points. The board should then be free for removal by easing upward off the screen tags, then rotated to enable the switch sliders to clear the front panel edge, and so withdrawn.

Reassembly is the reverse of this process.

(h) Removal of the Focus Intensity Graticule PCB
If it is necessary to gain access to the control pots proceed as follows. Remove the collet secured knobs on the control pots' shafts. The collet securing screws are beneath the knob cover cap. Unscrew the two screws holding the shield over the F.I.G. PCB. The PCB is now free and if the shield is moved away from the PCB the components on the PCB are accessible.

(j) Removal of the DSP PCB.

Unscrew all the fixing screws on the DSO and CPU boards, except the two which hold the DSO hinge support bar. Remove SKCC from the CPU board. Tilt up gently from the rear and unsolder the coaxial cable PLLL. Remove all plugs and sockets from the DSO PCB and unscrew the two screws on the hinge support bar. The DSO board can now be lifted clear of the instrument.

(k) Removal of the switch Pickoff PCB.

If access to the switch pickoff board is required for repair or maintenance, the DSO PCB must be removed first. When the board has been removed the area around the switch pickoff board will be clear. The switch pickoff board is supported by two pillars on the edge near the c.r.t. and the switch wafer on the opposite side. Unscrew the nuts securing the wafer onto the switch shaft, and slide the board off the two pillars and the switch shaft. The board can now be lifted clear.

(l) Removal of the cursor switch PCB.

To remove the cursor switch PCB it is necessary to remove the DSO PCB first. When clear unscrew securing the board to the inner front panel. The board can now be lifted clear.

(m) Removal of the CPU board.

To remove the CPU board it is necessary to remove the DSO PCB first. Unscrew the two fixing screws on the CPU board, these are situated on either side of the edge connector. The board can now be gently removed from the connector.

5.3 FAULT FINDING

Before any fault location is attempted, it is suggested that all supply voltages are checked. Subsequent signal voltages and waveforms should then be checked according to the following list, which may be used as a general guide and aid to servicing. Note that the typical voltages for unstabilised supplies are quoted for nominal mid-range supply voltages.

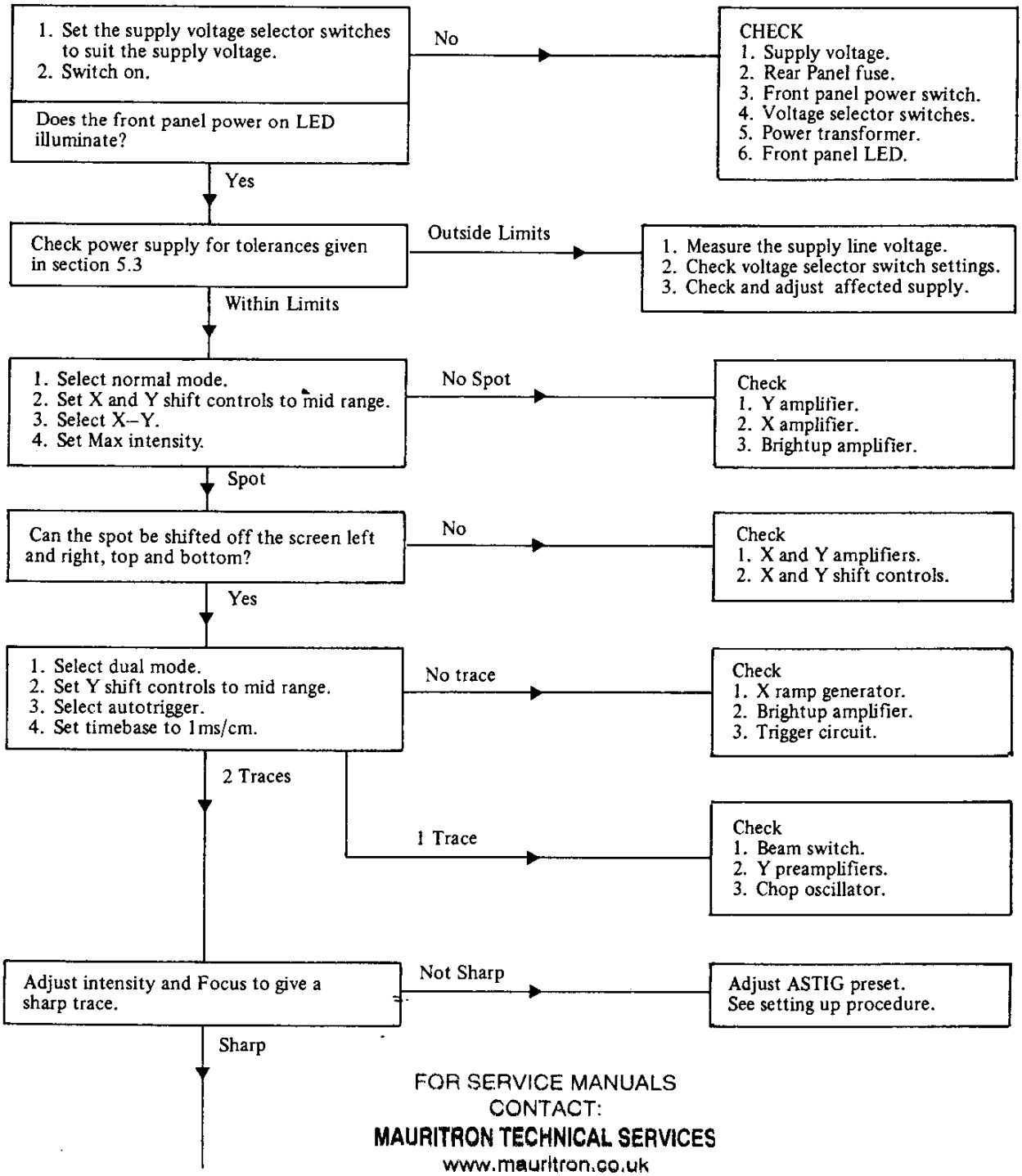
If a fault cannot be cleared it is recommend that the instrument is returned to the manufacturer for repair (see section 7).

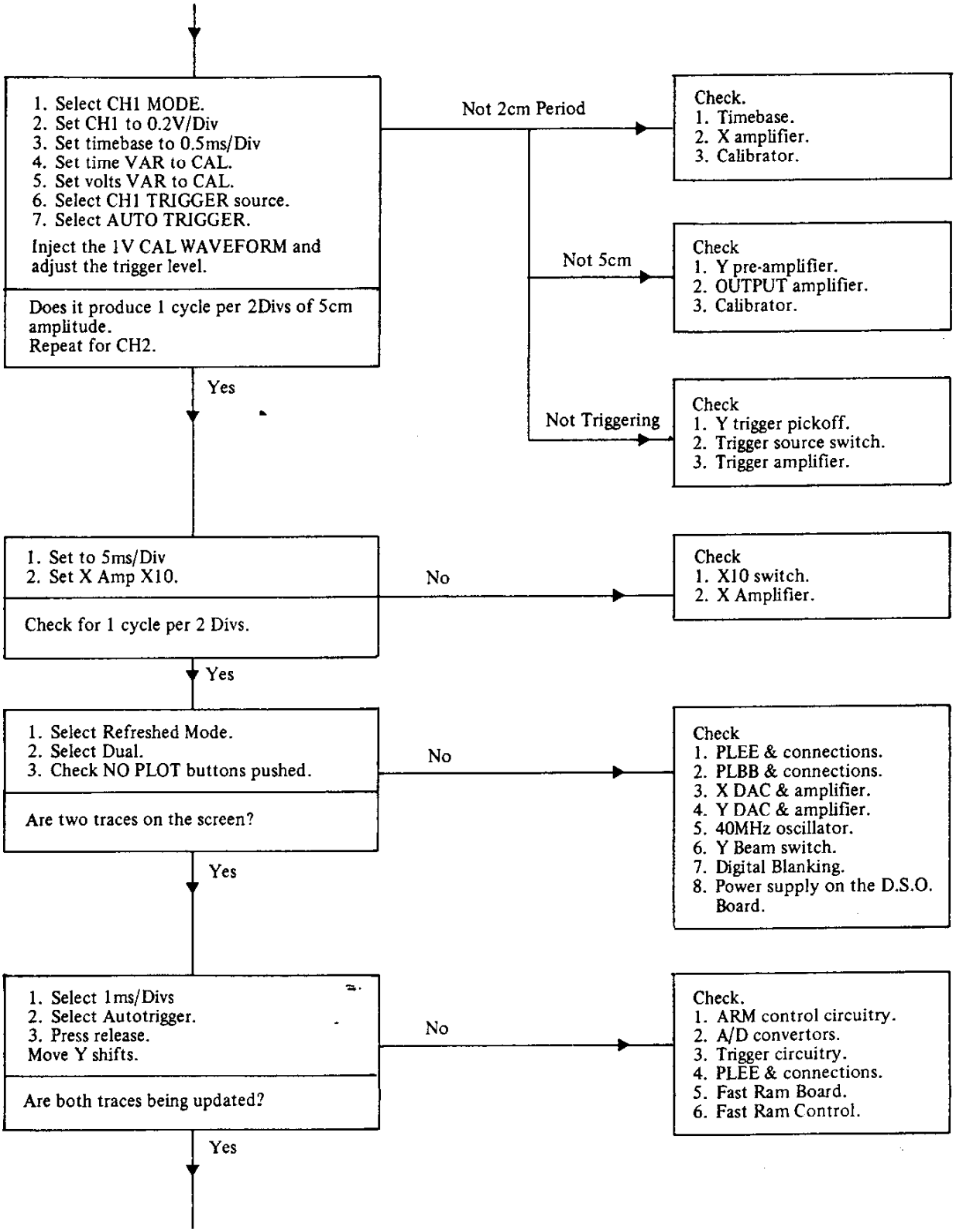
When faults have been cleared it is recommended that the setting-up procedure of section 5.4 is followed.

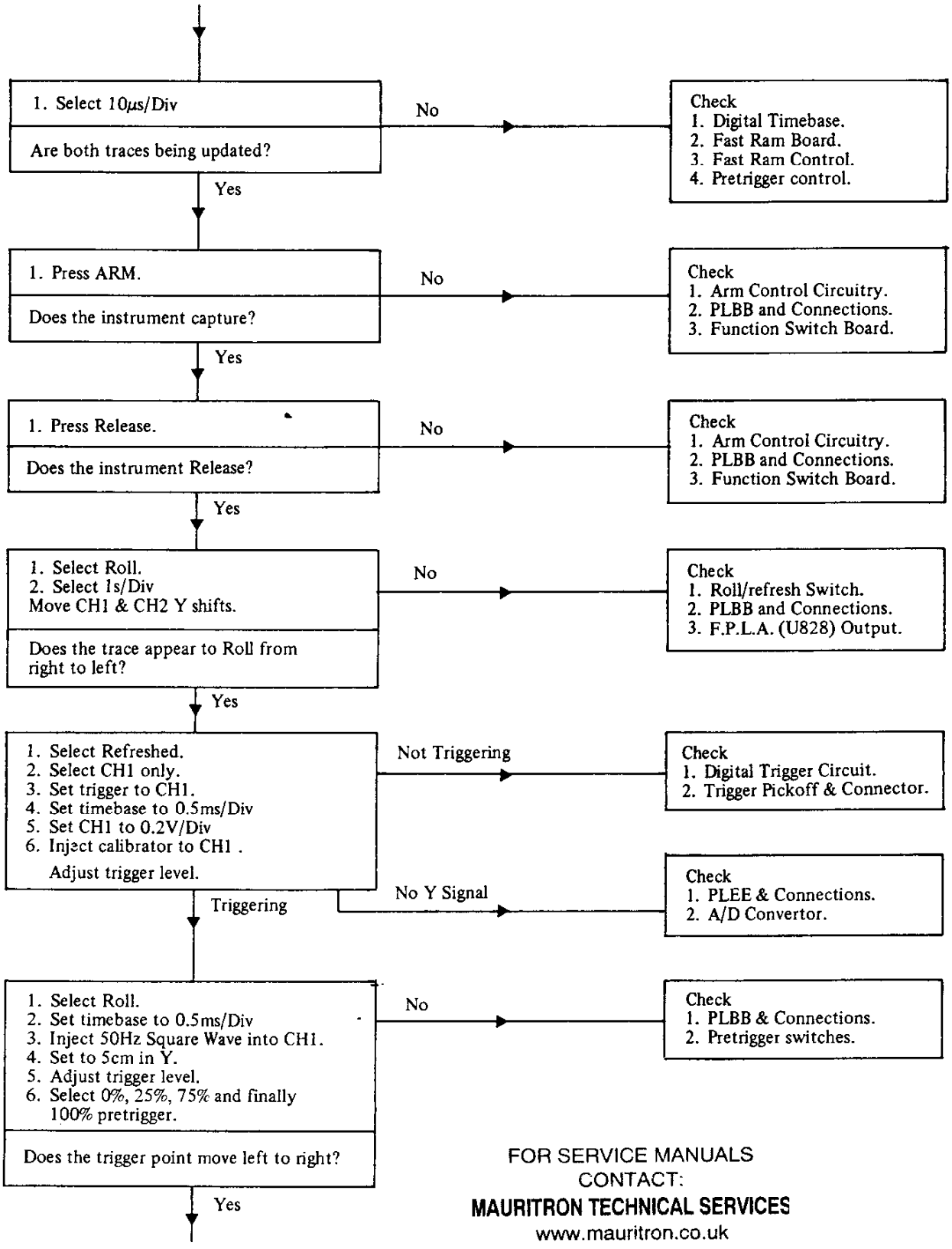
For checking the supply lines there is a double row of test pins, separated by bridged split pads. These pins will give outputs of +11V, −11V, +210V, +7V and −5V and if required the currents drawn by each line can quickly be measured simply by breaking the solder shorting the split pad for normal working operation, and inserting a current measuring meter between the two pins. In all five cases the line feed is nearer to the rear of the instrument, whilst the line load is connected to the forward pin.

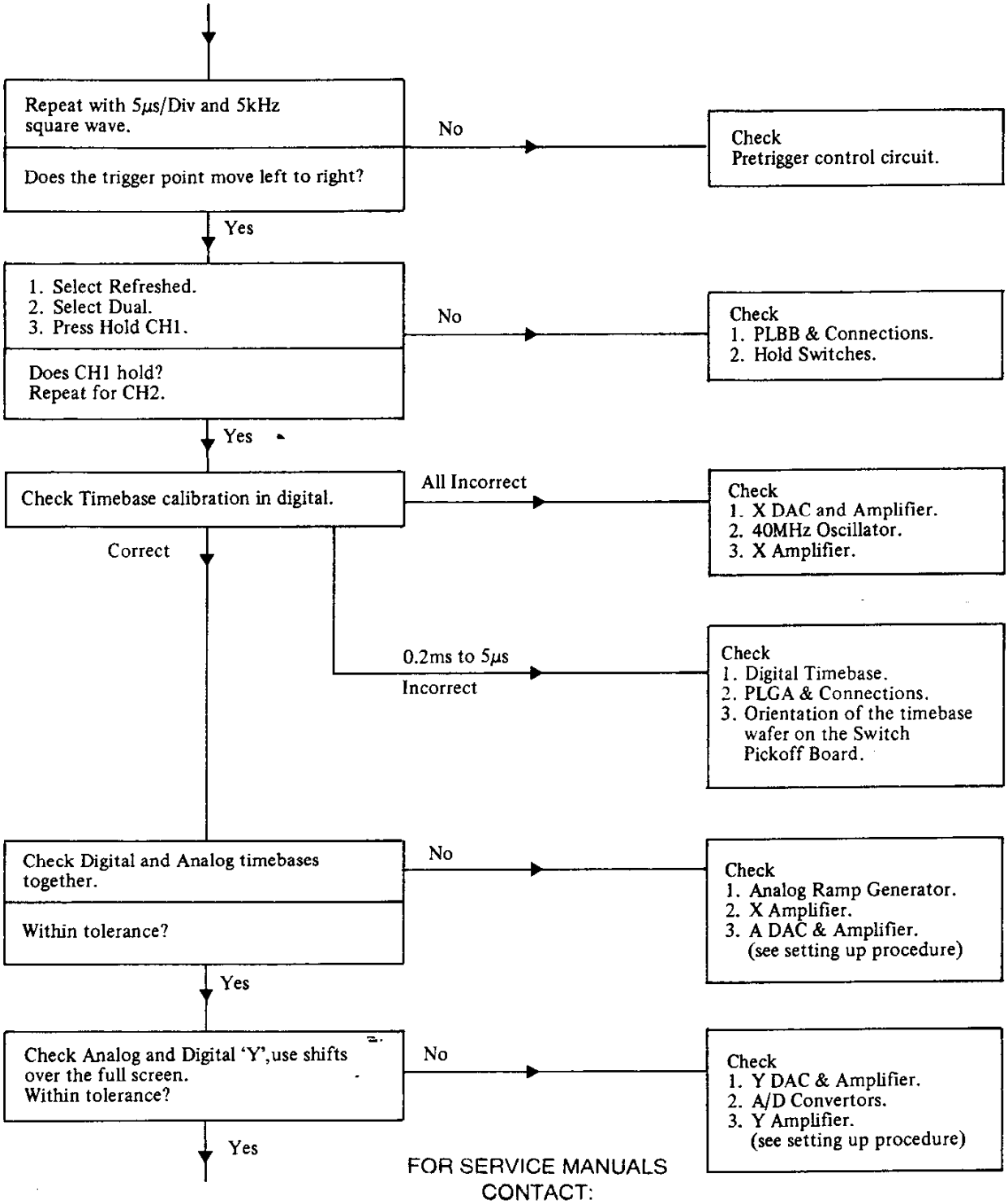
The fault finding tables define a suggested procedure to localise the fault to one particular area. Subsequent detailed guidance will be obtained from the relevant circuit diagram and circuit description and from the table of operating potentials.

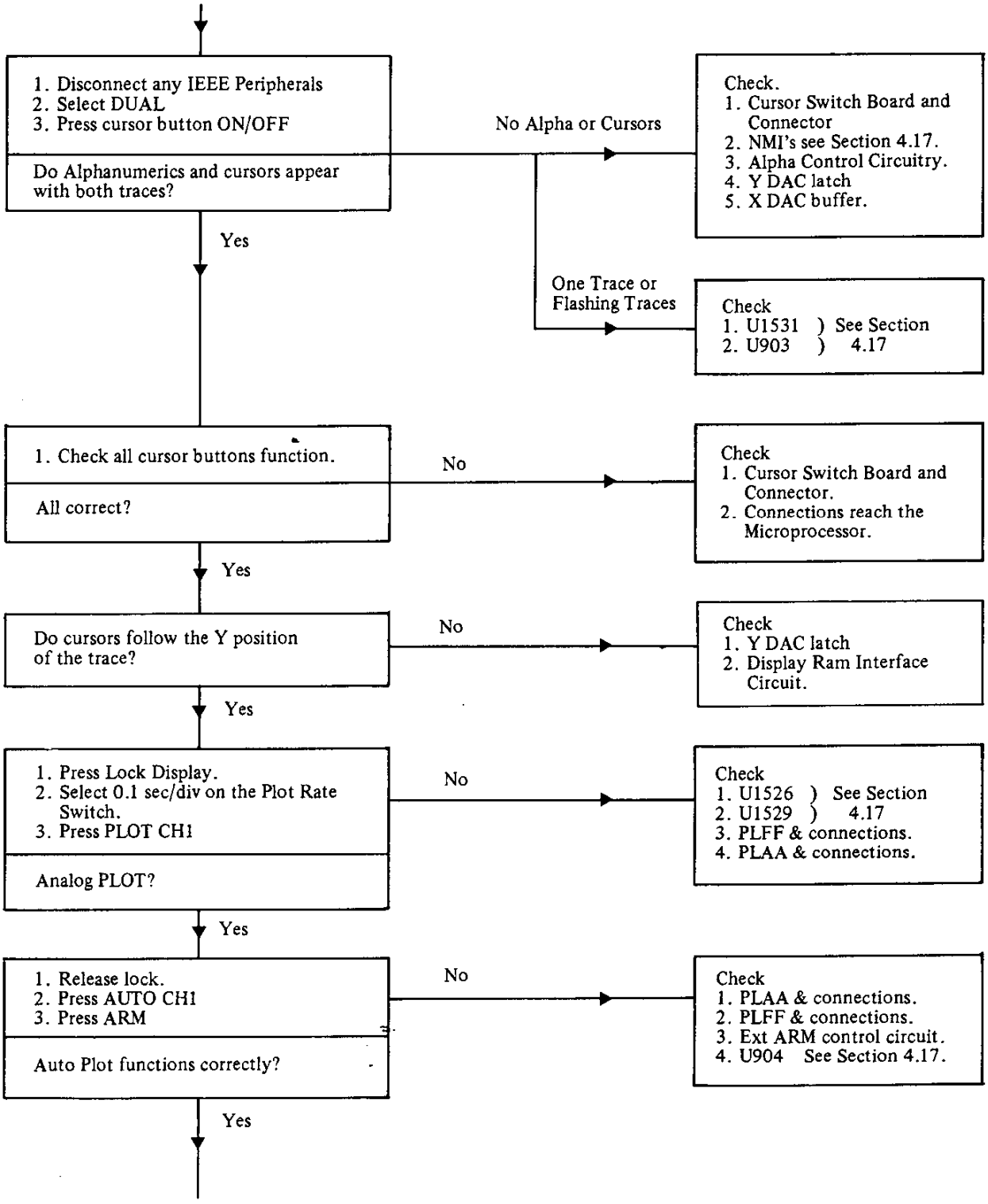
FAULT FINDING

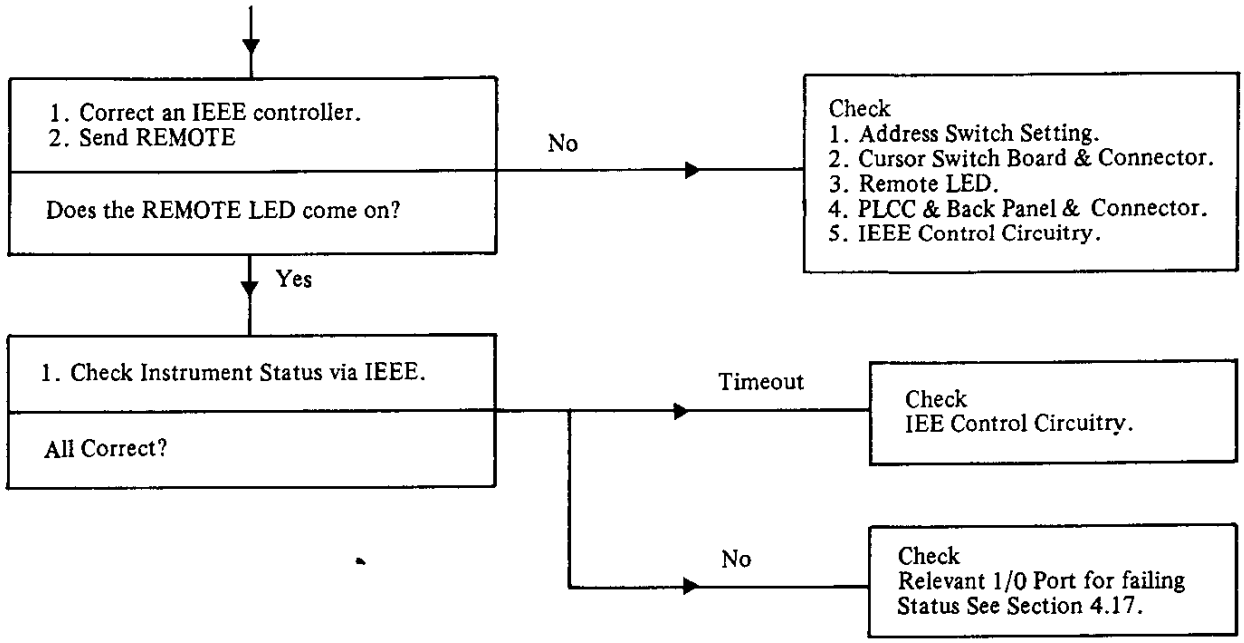



1. Select CH1 MODE.
2. Set CH1 to 0.2V/Div
3. Set timebase to 0.5ms/Div
4. Set time VAR to CAL.
5. Set volts VAR to CAL.
6. Select CH1 TRIGGER source.
7. Select AUTO TRIGGER.
Inject the 1V CAL WAVEFORM and adjust the trigger level.
Does it produce 1 cycle per 2Divs of 5cm amplitude.
Repeat for CH2.
Not 2cm Period
Check.
1. Timebase.
2. X amplifier.
3. Calibrator.
Not 5cm
Check
1. Y pre-amplifier.
2. OUTPUT amplifier.
3. Calibrator.
Not Triggering
Check
1. Y trigger pickoff.
2. Trigger source switch.
3. Trigger amplifier.
Yes
1. Set to 5ms/Div
2. Set X Amp X10.
Check for 1 cycle per 2 Divs.
No
Check
1. X10 switch.
2. X Amplifier.
Yes
1. Select Refreshed Mode.
2. Select Dual.
3. Check NO PLOT buttons pushed.
Are two traces on the screen?
No
Check
1. PLEE & connections.
2. PLBB & connections.
3. X DAC & amplifier.
4. Y DAC & amplifier.
5. 40MHz oscillator.
6. Y Beam switch.
7. Digital Blanking.
8. Power supply on the D.S.O. Board.
Yes
1. Select 1ms/Divs
2. Select Autotrigger.
3. Press release.
Move Y shifts.
Are both traces being updated?
No
Check.
1. ARM control circuitry.
2. A/D convertors.
3. Trigger circuitry.
4. PLEE & connections.
5. Fast Ram Board.
6. Fast Ram Control.
Yes






1. Disconnect any IEEE Peripherals
2. Select DUAL
3. Press cursor button ON/OFF
Do Alphanumerics and cursors appear with both traces?
No Alpha or Cursors
Check.
1. Cursor Switch Board and Connector
2. NMI's see Section 4.17.
3. Alpha Control Circuitry.
4. Y DAC latch
5. X DAC buffer.
Yes
One Trace or Flashing Traces
Check
1. U1531) See Section
2. U903) 4.17
1. Check all cursor buttons function.
All correct?
No
Check
1. Cursor Switch Board and Connector.
2. Connections reach the Microprocessor.
Yes
Do cursors follow the Y position of the trace?
No
Check
1. Y DAC latch
2. Display Ram Interface Circuit.
Yes
1. Press Lock Display.
2. Select 0.1 sec/div on the Plot Rate Switch.
3. Press PLOT CH1
Analog PLOT?
No
Check
1. U1526) See Section
2. U1529) 4.17
3. PLFF & connections.
4. PLAA & connections.
Yes
1. Release lock.
2. Press AUTO CH1
3. Press ARM
Auto Plot functions correctly?
No
Check
1. PLAA & connections.
2. PLFF & connections.
3. Ext ARM control circuit.
4. U904 See Section 4.17.
Yes



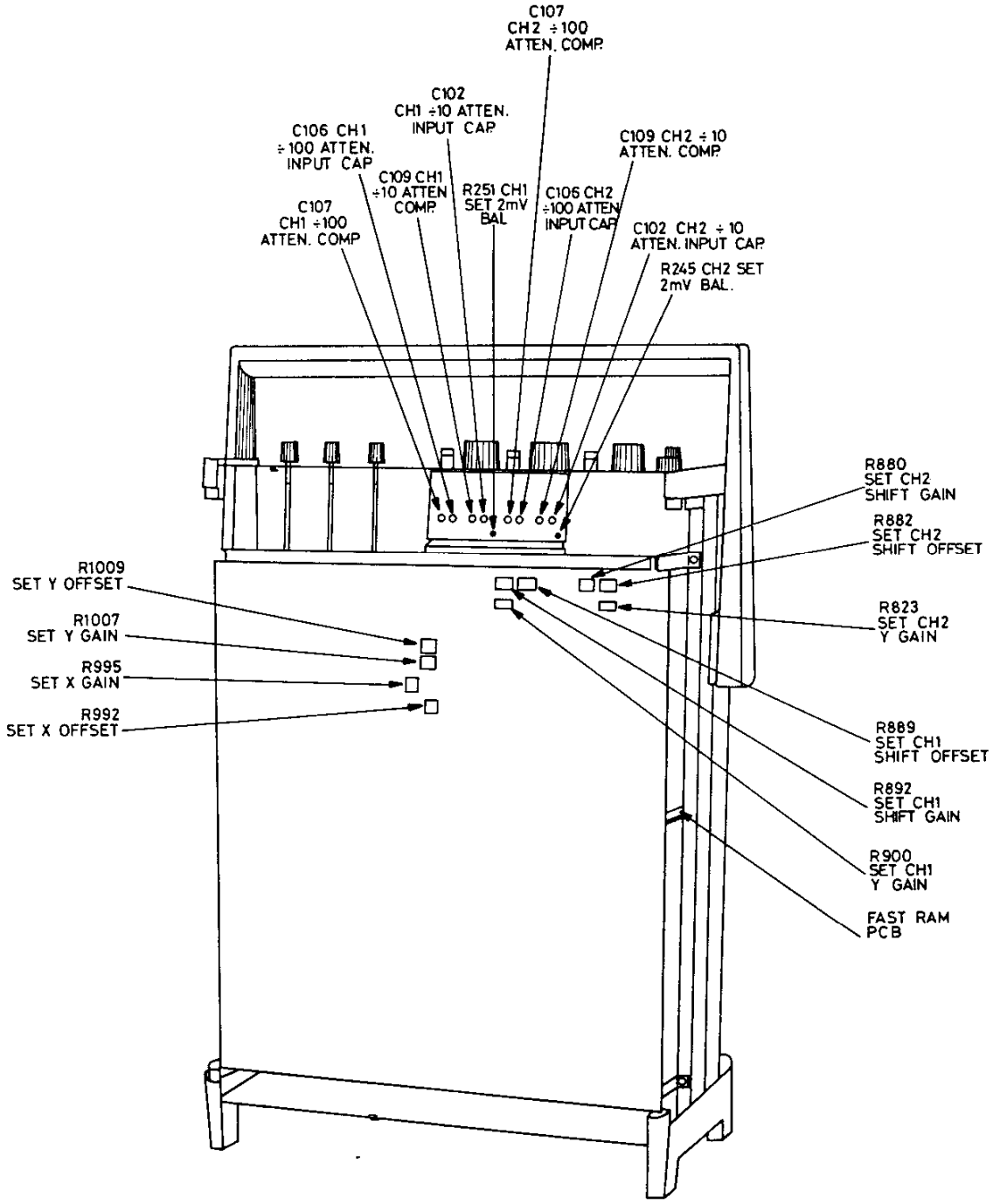


Fig. 4. Component Layout View

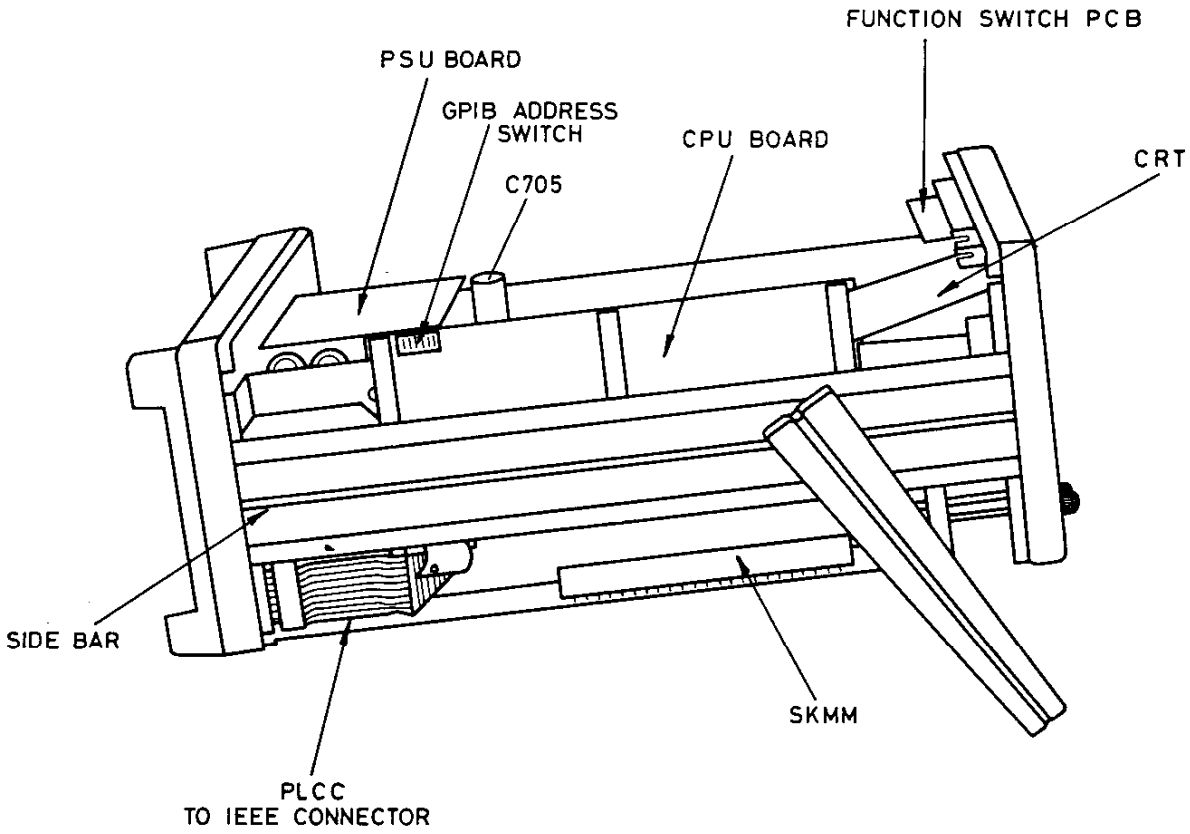


Fig. 5. Component Layout View

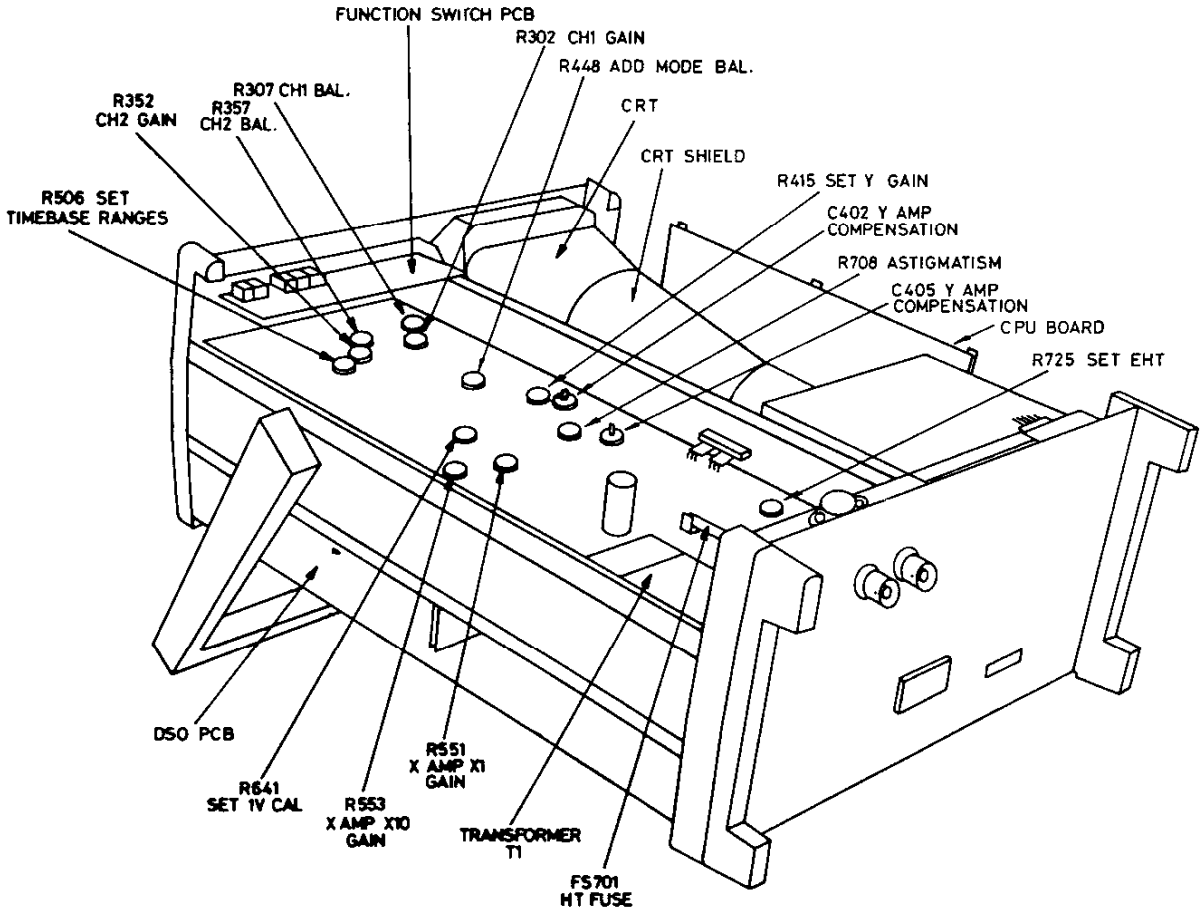


Fig. 6. Component Layout View

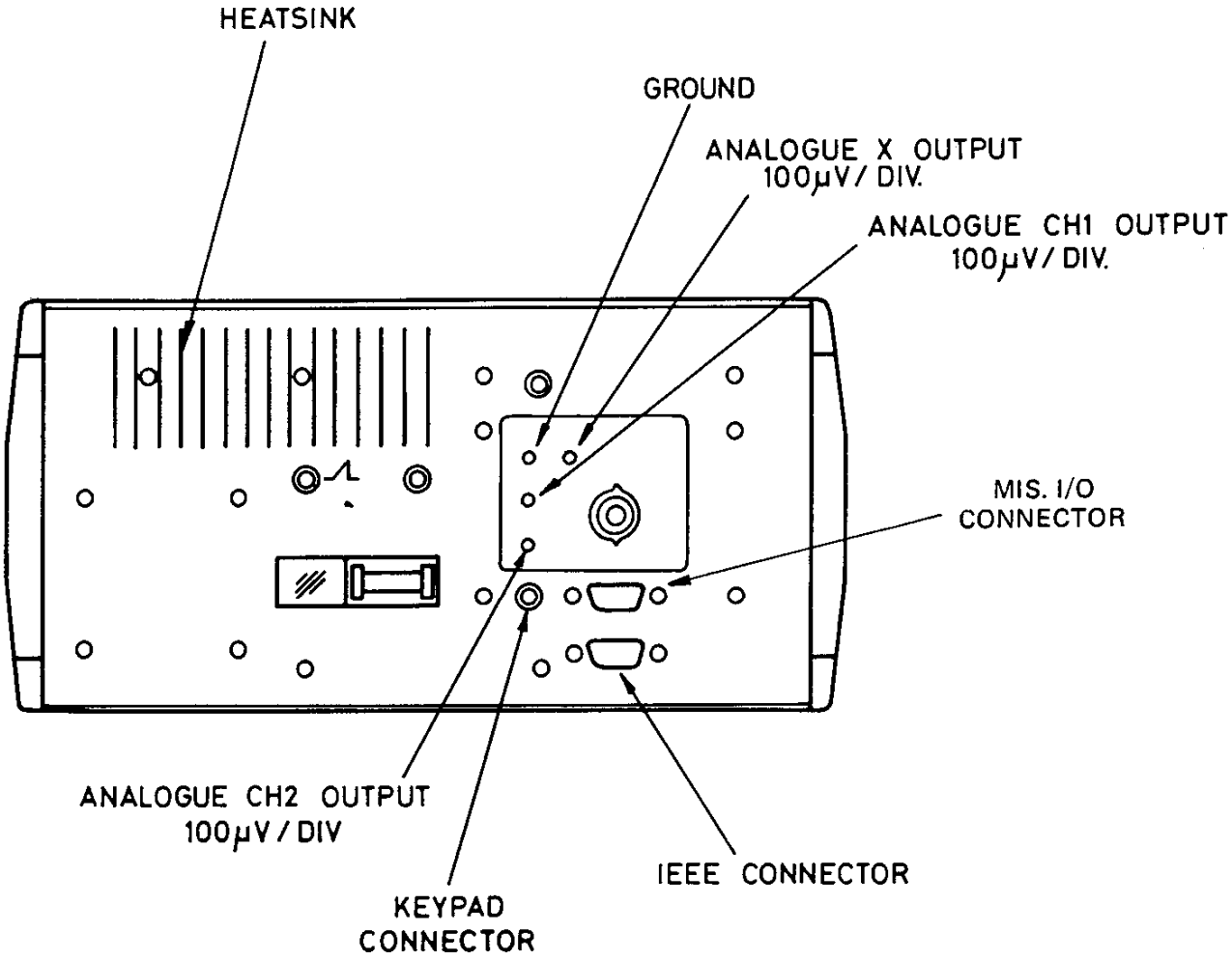


FIG. 7. BACK PANEL

Fig. 7. Component Layout View

(a) Supplies Unregulated.

268V DC	across C705 from 210 RMS Secondary voltage	
2.5kV DC	across C711 & C712 from 950V RMS Secondary voltage	
12.5V DC	across C1301 from 8.5V RMS Secondary voltage	
−12.5V DC	across C1304 from 8.5V RMS Secondary voltage	
18.5V DC	across C1309 from 13.5V RMS Secondary voltage	
19.0V DC	across C1311 from 13.5 RMS Secondary voltage	

Stabilised

+210V	±21V	
+ 11V	± 0.5V	Across C1313
+ 7V	± 0.4V	"
+ 5V	± 0.25V	Across C1306
− 5V	± 0.25V	Across C1307
− 11V	± 0.5V	Across C1314

(b) Y−Amplifier

Measurements for Ch1 only. Input to GND

Test Point		D.C. Level	
U201b	pin 8	0V	
U202a	pin 15	+0.2V	
	pin 1	+7V	
U202c	pin 9	-0.7V	
	pin 11	+1V	
U301d	pin 11	+3.7V	
U301b	pin 3	+3V	
TR401/402 Collector		+3.7V	40mV/cm each side
TR403/404 Collector		+7.7V	140mV/cm each side
TR405/406 Collector		+12.6V	-
TR4057/408 Base		+15.6V	-
TR407/408 Collector		+115V	6.8V/cm each side

(c) Analogue Ramp Generator

Test Point	Signal
Across R265 or R266	0.8V d.c. at "cal" 0.3V d.c. at min.
IC261 pin 3 and pin 6	+3.7V ramp from 0.1V level
TR264 Collector	+3.7V ramp from base level between 0 and +4V dependent on sweep rate selected.

(d) X-amplifier

Test Point	D.C. Level	Signal
TR512 Collector	+0.65V (Centre Screen)	500mV/cm 6.0V ramp
TR511 Emitter	+3.7V (Centre Screen)	500mV/cm 6.0V ramp
TR514	−3.0V	
TR513/513	+118V	12V/cm each side 140V ramp each side

(e) Trigger Amplifier

Test Point	D.C. Level	Signal
TR601/602 Base	0V on Ext. 0V on Int. A.C.	65mV/cm each side
	+3.5V on Int. D.C.	65mV/cm each side
TR601/602 Collector	−4.8V	25mV/cm each side

On TV mode:− TR601 and TR602 collector drops to between −8.5V and −10.5V dependent on the setting of the Trig. Level Control.

IC602, pin 9. Trigger output switches between −2V and −5.6V levels.

(f) Timebase Control

Test Point	Signal
IC501, pin 14	+5V, ±0.25V
IC501, pin 1	+5V (+1V at end of ramp)
IC501, pin 2	+4V (0V during hold-off)
IC501, pin 3	Trigger pulses between −0.5V and +2.8V levels
IC501, pin 4	+5V (0V during reset by bright-line)

Test Point	Signal
IC501, pin 5	+0.2V between sweeps +4.5V during sweeps
IC501 pin 6	+4.5V between sweeps +0.2V during sweeps
IC501, pins 8,9	Beam switched between +0.2V and +4.3V levels
IC501, pins 10, 13	−0.6V or 4.5V depending on mode switch setting.
IC501, pin 11	Chop/alt. pulses between +0.2V and +4.7V levels
IC601, pin 8	+0.5V triggered or bright-line off +0V bright line operating
IC601, pin 9	0V triggered or bright-line off +9.5V bright line operating

(g) Bright-Up Amplifier

Test Point	Signal
TR507 Collector	Switching signal +4.8V (Blank) to 0V (Bright up)
TR702 Base	+2
Collector	Between +6V and +48V dependent on intensity
RN720, pin 4	−2kV
RN720, pin 5	+50V with respect to pin 4
RN720, pin 6	+340V with respect to −1850V
Q832 Collector	0V Bright Up 2V Blank

(h) A/D Converter

Only signals for CHAN 1 shown.

Instrument in REFRESH Mode at 5μs/Div

Test Point		Signal
Q801,Q802	base	+3V
	collector	0V
Q804	base	−1.5V
	collector	+5V ±1V of signal
Q807	base	−3V
Q806	emitter	−1V ±1V of signal
U844	pin 8	0V to −2V sampled signal
Q809	base	0V
U843	pin 21	−1V ±1V of signal
U843	pin 28	−2V
U840	pin 1	−5V to +2V
U811,Q812	base	ECL level 10ns pulse every 50ns
	collector	+8V 10ns pulse every 50ns
U847	pin 3	ECL level 10ns pulse every 50ns
U846	pins 9&10	20MHz clock. ECL LEVEL

(i) DIGITAL Timebase

Instrument in REFRESH mode at 5μs/Div

Test Point		Signal
U835	pin 3	40MHz TTL
U835	pin 5	20MHz TTL
U823	pin 1	10MHz 50% Mark/space
	pin 2	1MHz 20% M/S
	pin 3	20MHz 50% M/S
	pin 4	2MHz 33% M/S
	pin 12	200KHz 80% M/S
	pin 13	ULA Timebase
	pin 14	5MHz 50% M/S
	pin 15	500KHz 50% M/S
U910	pin 54	2MHz TTL

(j) Store Control

Instrument in REFRESH mode at 0.5ms/Div

Test Point		Signal
U831	pin 46	TTL High
	pin 48	200KHz clock even M/S
	pin 47	Two 250ns Negative going Pulses every 5μs.
	pin 47	1 during RAMP 0 during Hold Off
	pin 52	20μs positive going pulse every 5ms.
	pin 18	5μs negative going pulse every 5ms.

(k) Digital to Analog Converter

Instrument in REFRESH mode at 0.5ms/Div

Test Point		Signal
U862	pin 11	200KHz clock
U861	pin 13	+6.2V
U860a	pin 1	3.9V DC Sensitivity 70mV/cm.
U860d	pin 14	3.9V DC Sensitivity 70mV/cm

(l) Digital Ramp Generator

Instrument in REFRESH mode at 0.5V/Div

Test Point		Signal
U910	pin 23	200Hz clock with even Mark/Space
U910	pin 45	200KHz clock with even Mark/Space
U864	pin 1	200Hz RAMP from 0V to +3.5V

(m) CPU Board

During power up.

Test Point		Signal	
U1501	pin 6	0V slow ramp to +5V.	
U1501	pin 8	CMOS low	With U1501 pin 6
U1501	pin 9	CMOS low	< 0.7V
U1501	pin 10	CMOS high	

After power up

U1501	pin 40	1MHz CMOS	U1538	pin 9	200KHz CMOS
U1501	pin 4	5ms TTL low, 10ms TTL high	U1536	pin 13	2MHz CMOS
U1545	pin 9	250KHz CMOS	U1529	pin 7	between –0.4V and +0.4V
U1538	pin 1	5μs negative going pulse every 5ms.	U1529	pin 14	between –0.4V and +0.4V

(n) F.P.L.A. U828

	INPUTS								OUTPUTS					
Range	D0	D1	D2	D3	D4	S2	S5	T	RSS	Div2	Div5	D1	D2	Div1K
50s/Div	0	0	0	0	1	0	0	0	0	1	0	0	0	0
20	0	0	0	1	0	1	0	0	0	0	1	0	0	0
10	0	0	0	1	0	0	1	0	0	0	0	1	0	0
5	0	0	0	1	0	0	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	0	0	0	1	1	0	0
1	0	0	1	0	0	0	1	0	0	0	0	0	1	0
0.5	0	0	1	0	0	0	0	0	0	1	0	0	1	0
0.2	0	1	0	0	0	1	0	0	0	0	1	0	1	0
0.1	0	1	0	0	0	0	1	0	0	0	0	1	1	0
50ms/Div	0	1	0	0	0	0	0	0	0	1	0	1	1	0
20	1	0	0	0	0	1	0	0	0	0	1	0	0	1
10	1	0	0	0	0	0	1	0	0	0	0	1	0	1
5	1	0	0	0	0	0	0	0	0	1	0	1	0	1
50	0	0	0	0	1	0	0	1	0	1	0	0	0	1
20	0	0	0	1	0	1	0	1	0	0	1	0	0	1
10	0	0	0	1	0	0	1	1	0	0	0	1	0	1
5	0	0	0	1	0	0	0	1	0	1	0	1	0	1
2	0	0	1	0	0	1	0	1	0	0	1	1	0	1
1	0	0	1	0	0	0	1	1	0	0	0	0	1	1
0.5	0	0	1	0	0	0	0	1	0	1	0	0	1	1
0.2	0	1	0	0	0	1	0	1	1	1	0	0	1	1
0.1	0	1	0	0	0	0	1	1	1	1	0	0	1	1
50μs/Div	0	1	0	0	0	0	0	1	1	1	0	0	1	1
20	1	0	0	0	0	1	0	1	1	1	0	0	1	1
10	1	0	0	0	0	0	1	1	1	1	0	0	1	1
5	1	0	0	0	0	0	0	1	1	1	0	0	1	1
pin no.	20	21	22	23	24	25	26	27	16	10	11	12	13	15

1 represents TTL High
0 represents TTL Low

5.4 SETTING UP PROCEDURE

The following procedure details the adjustments necessary to recalibrate the 4035 and set all the preset controls to achieve the specified performance. Inability to make these adjustments or failure to meet the specification after these adjustments have been made, should be considered as a fault and the operating conditions should be checked according to Section 5.3.

Set the Instrument initially to the NON STORAGE mode.

(a) Test Equipment

1. Multirange Test Meter including 2.5kV capability at 20kΩ/Volt.
2. Variable Autotransformer, output voltage 100-270V at 5A.
3. Sine/Square wave signal generator 10Hz to 100kHz, 20mV to 5V.
4. Source of Voltage and Time Calibration signals, such as Bradley Oscilloscope Calibrator type 192.
5. Square Wave Generator at 500kHz, 100mV amplitude into 50Ω, rise time less than 50ns with square corner and flat top.
6. RF Sinewave Constant Amptitude Signal Generator 25mV to 5V/pk to pk, 50kHz to 20MHz.
7. 10:1 Passive probe.

(b) Set E.H.T.
Set the incoming a.c. supply via the auto transformer to the nominal centre voltage of the selected range. Set to mid brilliance on the c.r.t. Monitor the collector voltage of Q707. Adjust R725 for this voltage to be 405V ±5V. Remove the voltmeter. The instrument may now be operated directly from the uncontrolled supply.

(c) Set Intensity Range
Set to X-Y mode with inputs grounded and centre the spot on the screen. Monitor the collector voltage of Q702. Adjust the intensity control for this voltage to be +15V, and then adjust R713 for the intensity to be near cut-off. Remove the voltmeter.

(d) Astigmatism
Display a mid frequency sinusoidal signal in the normal sweep mode on one channel, approx. 2Div pk to pk, and 4Div period. Set the VARiable sensitivity control fully anti-clockwise. Set to a fairly low brilliance and adjust both the focus control and R708 (Astig) for the sharpest trace over the whole of its length. Reset the VARiable sensitivity to CAL.

(e) Trace Rotation
Ground the inputs and set the horizontal trace to the centre line. Adjust the Trace Rotation preset to align the trace with the centre graticule line.

(f) Timebase Calibration
Ensure that the VARiable sweep is set to the CAL position. Apply 0.1ms calibrated markers to either channel input. Set the timebase to 0.1ms/Div. and obtain a triggered trace. Apply X10 Magnification and set R553 for 10Div spacing between the time markers.

Return to X1 Magnification and set R551 for 1cm spacing

Apply 1ms/Div markers and set the timebase to 1ms/Div. Set R506 for 1cm spacing between the time markers. All other timebase ranges can be checked for accuracy.

(g) X-Y Calibration
Ensure that the CH1 VARiable sensitivity control is set fully clockwise to CAL. Select X-Y and apply a calibrated 100mV square wave to Channel 1 Input. Select 20mV/Div on CH1, and ground CH2 input. Set R302 for 5cm horizontal trace length.

(h) Channel 1 Calibration
Select CH1. With a 100mV input of 20mV/Div, set R415 for a 5cm vertical amplitude signal. All other sensitivity ranges can be checked for accuracy.

(i) Ensure that the CH2 VARiable sensitivity control is set to the CAL. position. Transfer the 100mV calibration signal to CH2, and set to display that channel at 20mV/Div. Set R352 for a 5cm vertical amplitude signal.

All other sensitivity ramps can be checked for accuracy.

(j) Input Balance
Select CH1 and with input grounded adjust the preset Balance pot for no vertical movement of the trace between the 100mV/Div and the 5mV/Div ranges. Repeat for CH2.

(k) Trigger Balance
Set R357 for no vertical movement of the CH2 trace when Invert is selected. Connect a sinusoidal input, AC coupled, to CH1 and set the trace for about 5Div pk-pk signal, with one cycle displayed. Adjust R307 such that there is no change of trigger point as the TRIGGER Coupling is switched between AC and DC. Note that the relevant Shift control may have to be operated to return the trace to the centre of the screen when R307 or R357 is adjusted.

(l) 2mV/Div Balance
Set CH1 input VARiable sensitivity control to CAL position. Set CH1 input sensitivity to 5mV/Div and ground the input to CH1. Adjust R215 so that the trace does not shift as the CH1 sensitivity is

switched between 2mV/Div and 5mV/Div. Repeat for CH2, adjusting R2.

(m) Add Balance
Ground the inputs to CH1, and CH2 and select DUAL display mode. Using the POSITION centre both traces on the screen. Switch to ADD and adjust R448 to centre the trace on the screen.

(n) Attenuator Compensation
Apply a square wave input to CH1 at approx. 1V pk-pk and 1kHz. Select 0.2V/Div and adjust C109 on the CH1 attenuator assembly to obtain a square topped displayed pulse. Access is through the trim tool hole in the preamplifier screen.

Apply a square wave input to CH1 at approximately 10V pk-pk and 1kHz. Select 2V/Div and adjust C107 on the CH1 attenuator assembly to obtain a square topped displayed pulse.

Repeat for CH2.

(o) Input Capacitance Equalisation
Select 100mV on CH1 with the VARiable Sensitivity control set fully anti-clockwise and monitor a 10V 1kHz square wave via a 10:1 probe. Adjust the capactive compensation of the probe for a flat topped displayed pulse. Select 200mV/Div, reset the VARiable sensitivity to the CAL position, and adjust C102 for a similar Flat top to the pulse.

Select 2V/Div on CH1 with the VARiable Sensitivity control set to the CAL position and monitor a 100V square wave input. Adjust C106 for a flat top to the pulse.

Repeat for CH2.

(p) Pulse Response and Bandwidth
Monitor a fast rise square wave input signal to examine the edge in detail on the 20mV/Div and 0.5µs/Div ranges.

Adjust C405 for a flat top following the transition and C402 for the optimum corner to the pulse.

Connect a constant amplitude sinusoidal generator and set the input for 5cm pk to pk at 50kHz. Increase the frequency and check that the loss of amplitude is less than 3dB at 20MHz (3.5cm pk to pk).

(q) Calibrator
Monitor a calibrated 1V pk to pk square wave input and set the sensitivity and variable sensitivity controls for a full 8cm pk to pk display. Disconnect the external input and connect the Y input to the 4030 Calibrator output. Adjust R641 for a similar 8cm signal amplitude.

(r) Y ADC Adjustment
Select Refresh mode, cursors, 0.5ms/DIV sweep rate and set the display mode to CH1. Apply a 500mV square wave signal to CH1 and select an input attenuator setting of 100mV/div. Set one cursor on a high level and one as a low. Adjust R900 so the cursor readout displays 500mV. Repeat for CH2 adjusting R823.

(s) Y DAC Adjustment
With the settings as in (r) adjust R1007 so that the displayed signal is 5cm amplitude. Select 50mV/div and adjust R1009 so that the trace limited evenly top and bottom of the screen.

(t) Digital Shift Offset and Gain Adjustment
Set CH1 input coupling switch to GND. Ensure CH1 Trigger is selected and AUTO is on. Select NON STORAGE mode, and 0.5ms/Div sweep rate. Adjust the CH1 Position control to centre the trace on the screen. Select REFRESH mode. If a trace displacement occurs adjust R892 to bring the trace back to the centre of the screen. Switch back to NON STORAGE and set the trace to the upper edge of the screen. Select REFRESH and adjust R889 to bring the trace to the upper edge of the screen, if necessary. Repeat this process until no trace displacement occurs when switching between NON STORAGE and STORAGE modes.

Repeat for CH2 adjusting R881 and R880 respectively.

(u) Digital Timebase Adjustment
Select REFRESH mode, and a sweep rate of 0.5ms/Div. Apply time markers at 0.5ms rate. Adjust R995 so that the markers occur at 1Div intervals. Then switch between NON STORAGE and REFRESH, adjusting R992 so that the trace does not have an X displacement between NON STORAGE and REFRESH.

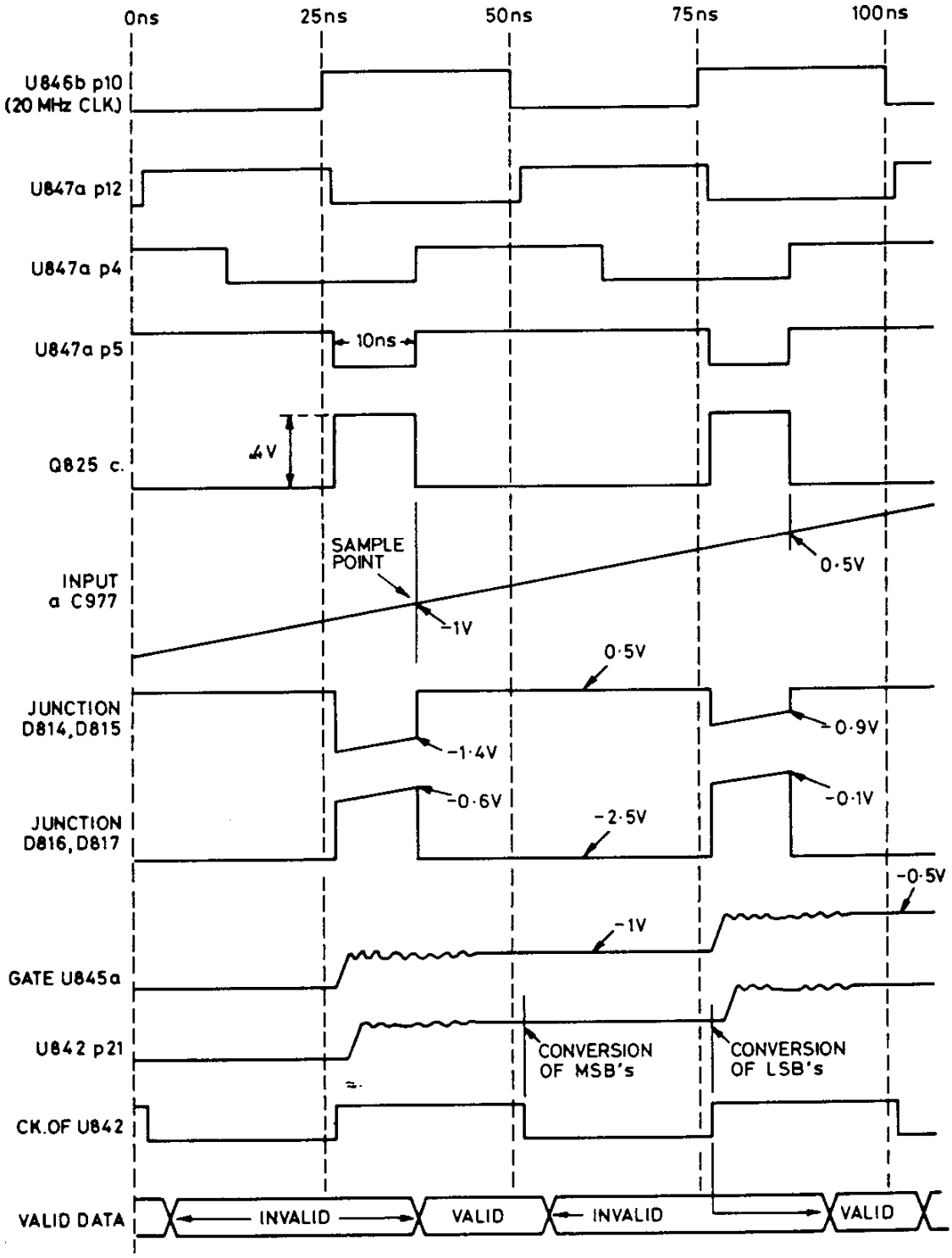


Fig. 8. A–D Timing Diagram

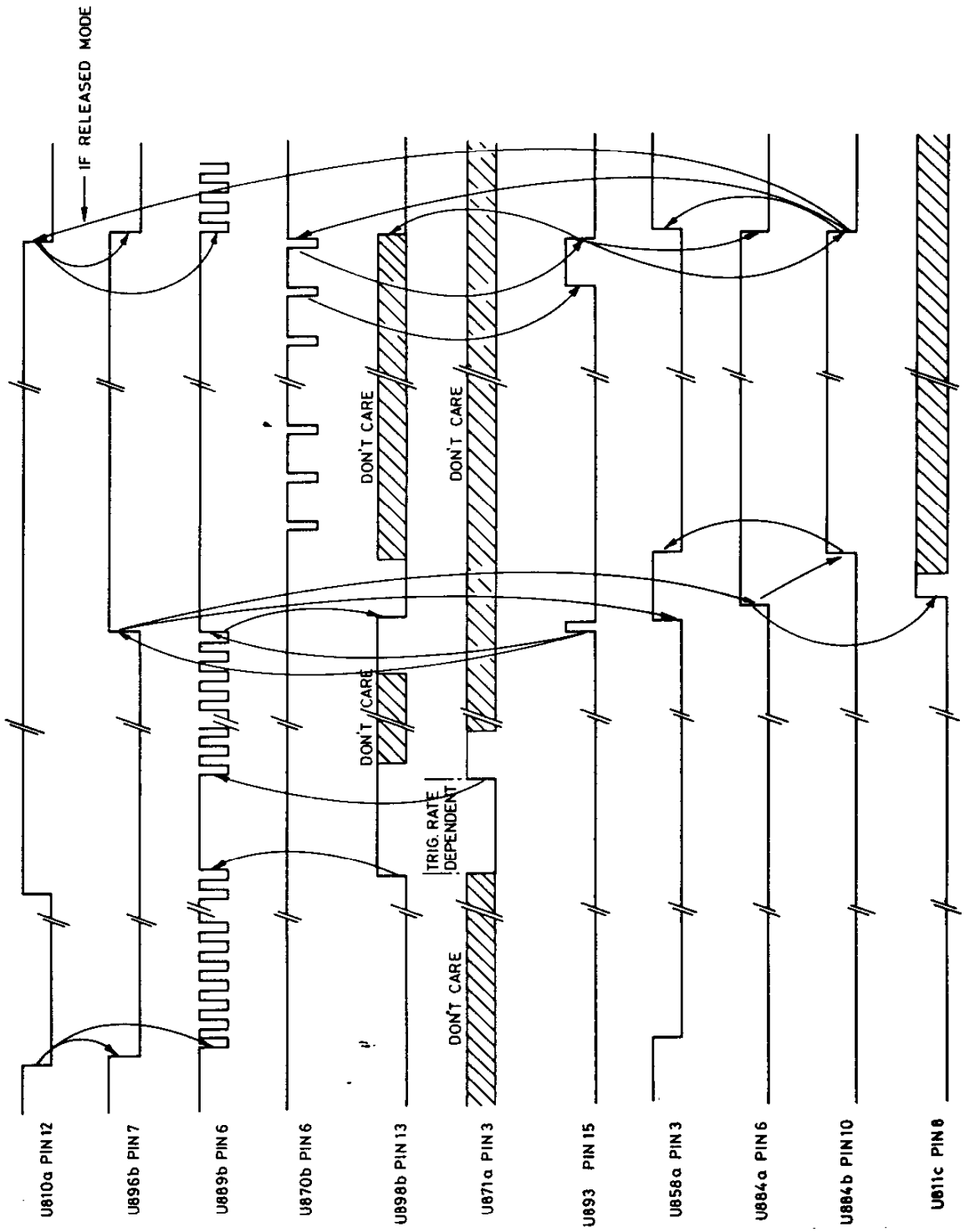


Fig. 9. Pre-trigger Timing Diagram 25% or 75% pre-trigger

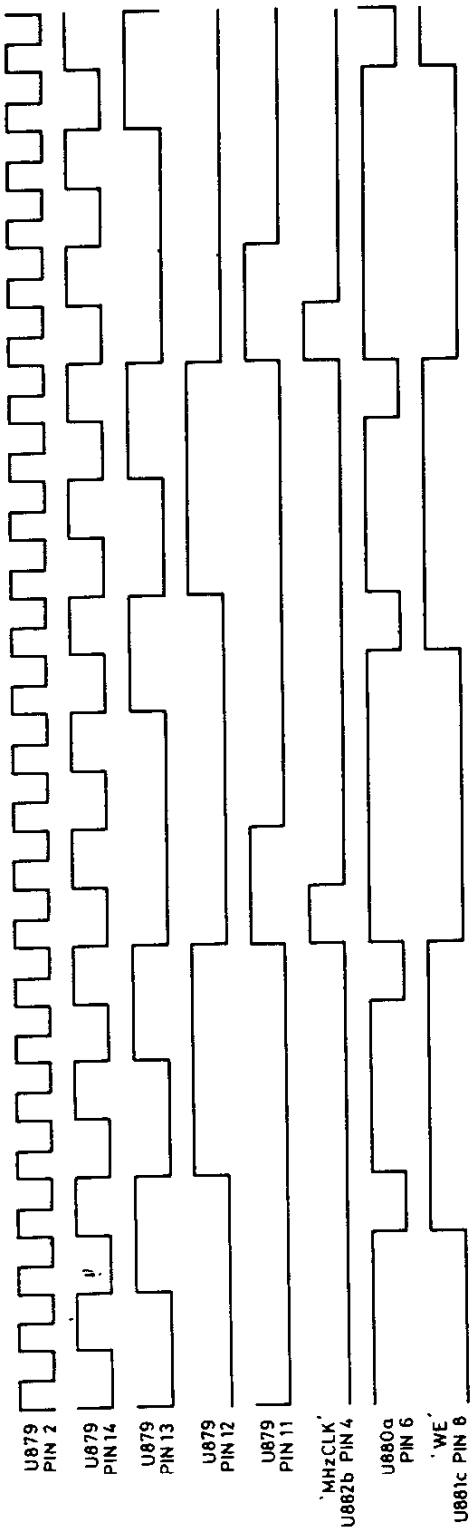


Fig. 10. U.L.A. Clock Generation Timing Diagram

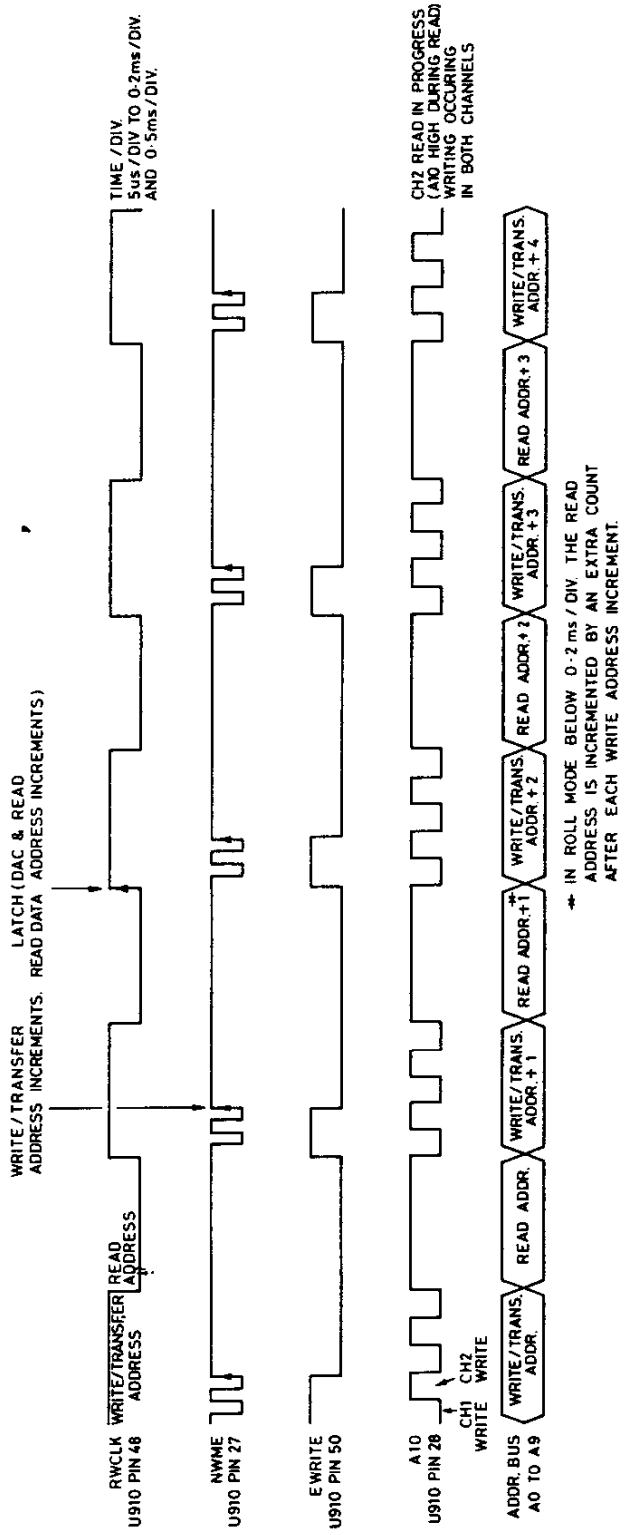


Fig. 11. Write/Transfer Timing Diagram

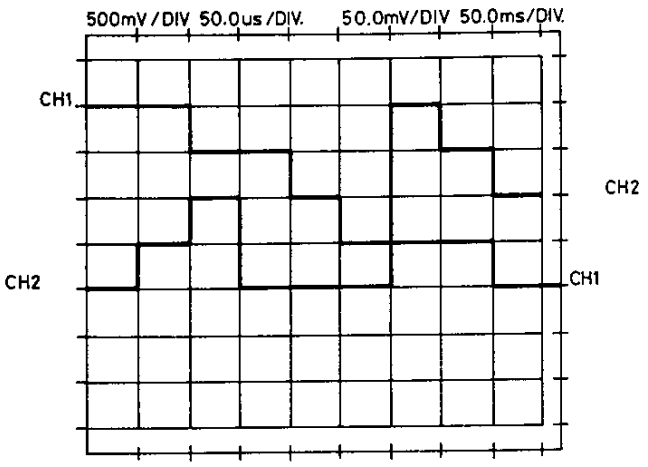


FIG. 12a

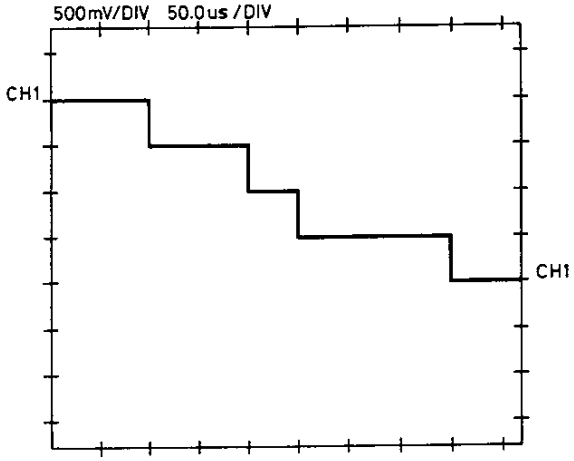


FIG. 12b

Fig. 12. GPIB Digital Plot Example

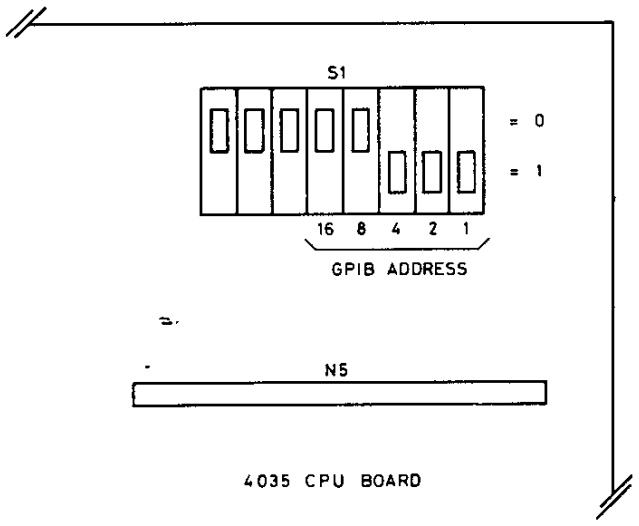


Fig. 13. GPIB Address Switch

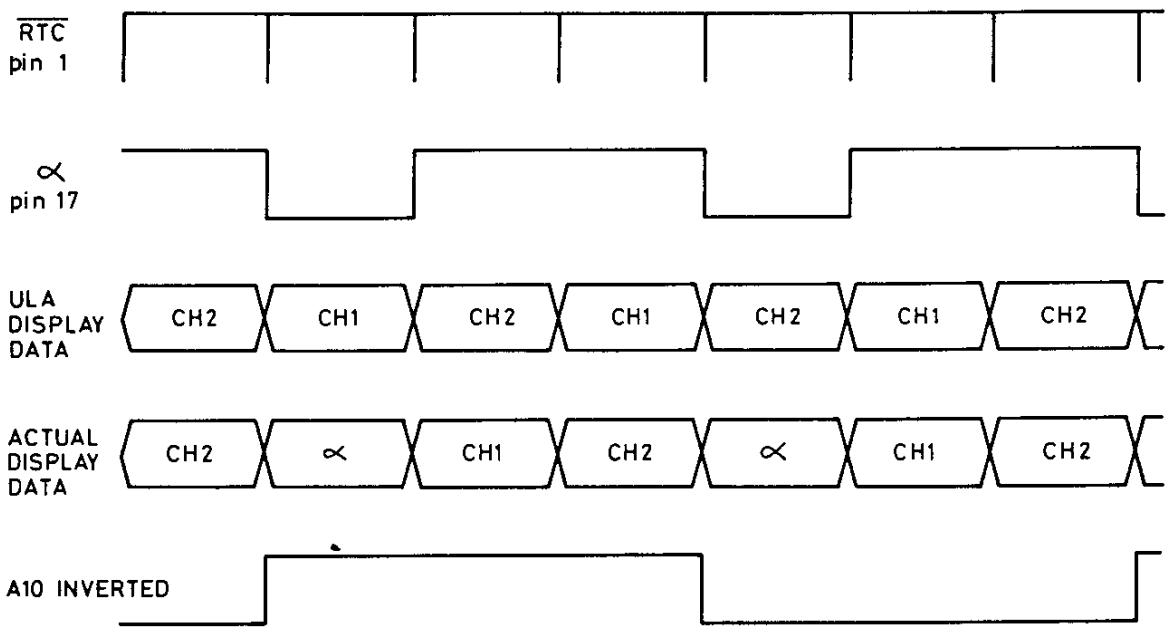


Fig. 14. PAL Timing Diagram

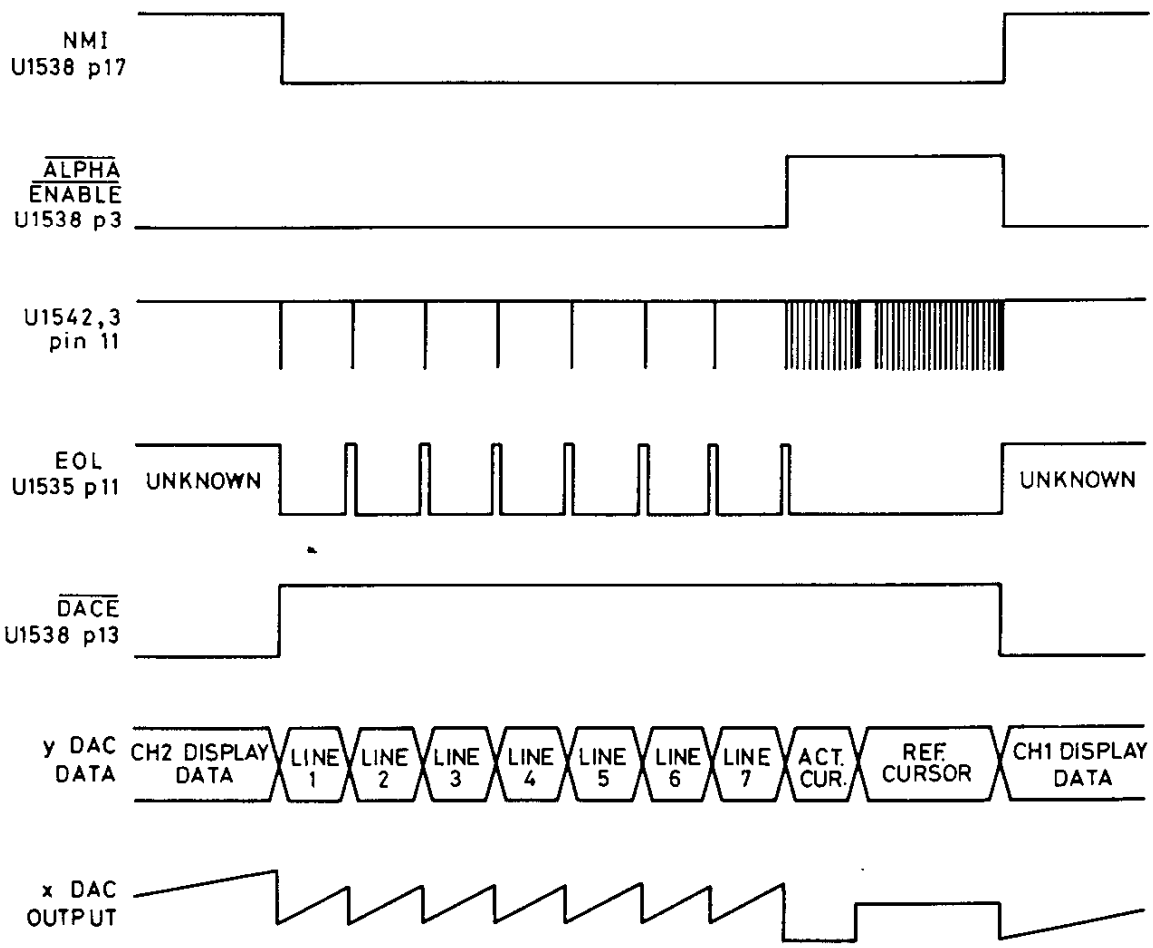


Fig. 15. Alphanumerics and Cursor Display Timing

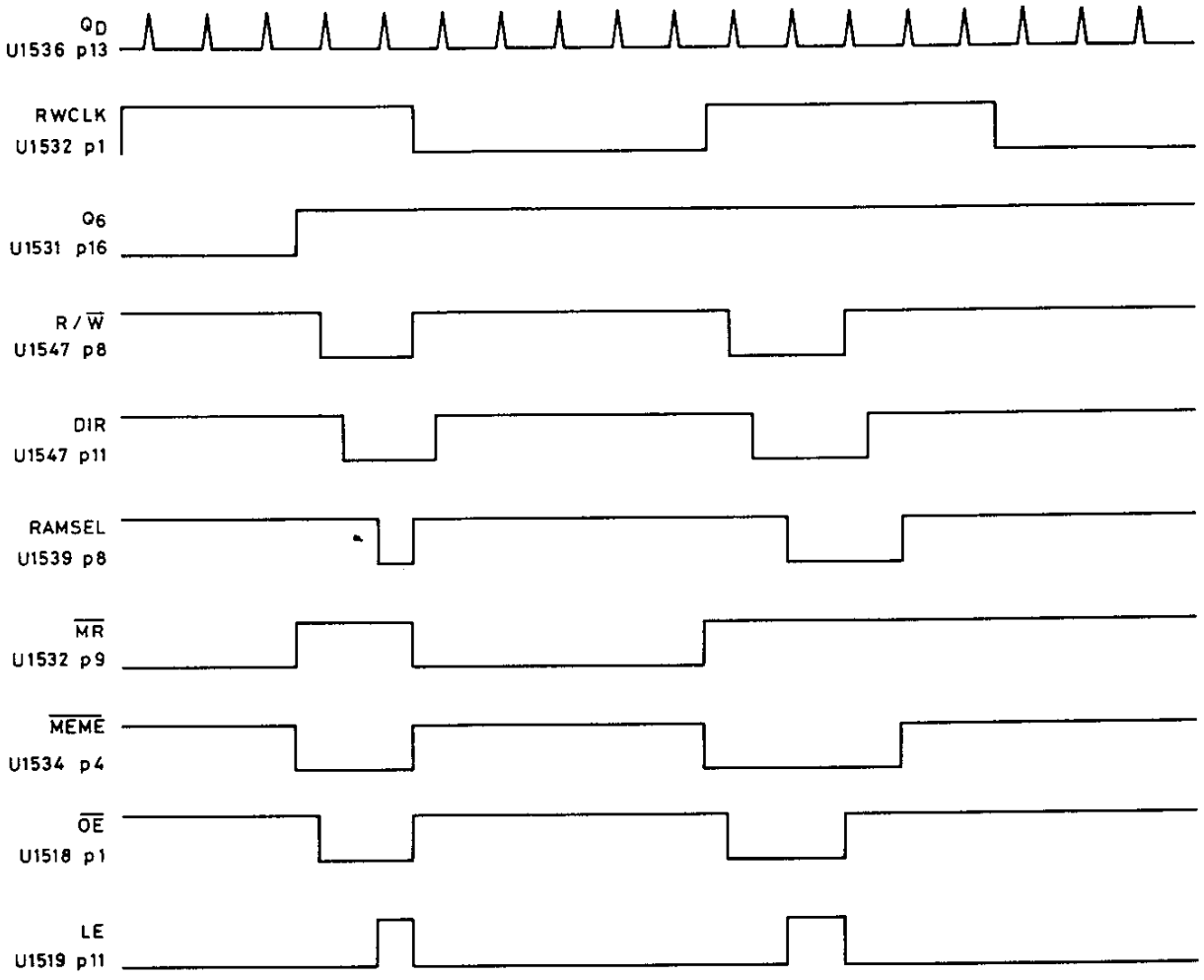


Fig. 16. CPU to DSO RAM Interface Timing Diagram

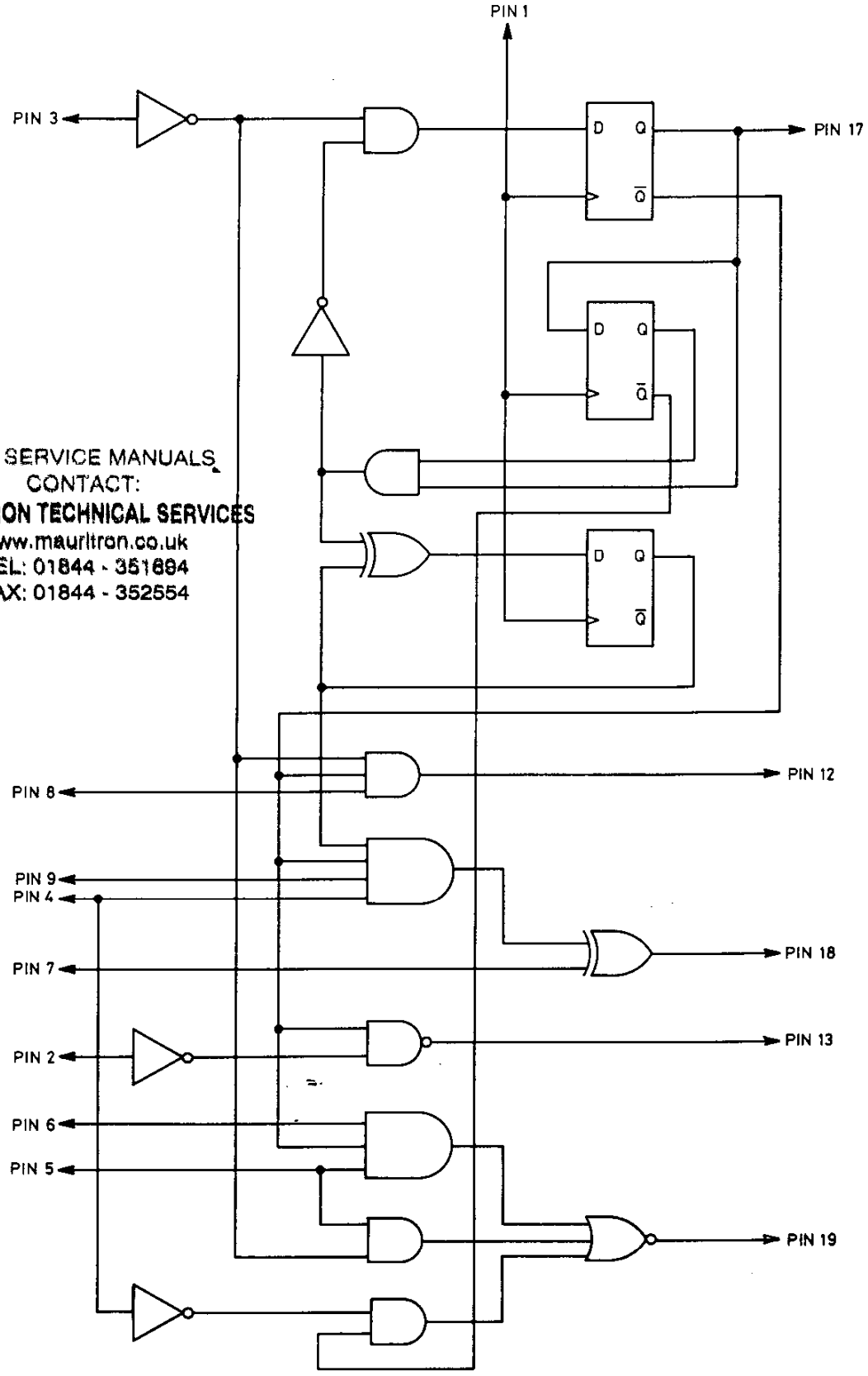


Fig. 17. Internal Functional Diagram of the PAL

ABBREVIATIONS USED FOR COMPONENT DESCRIPTIONS

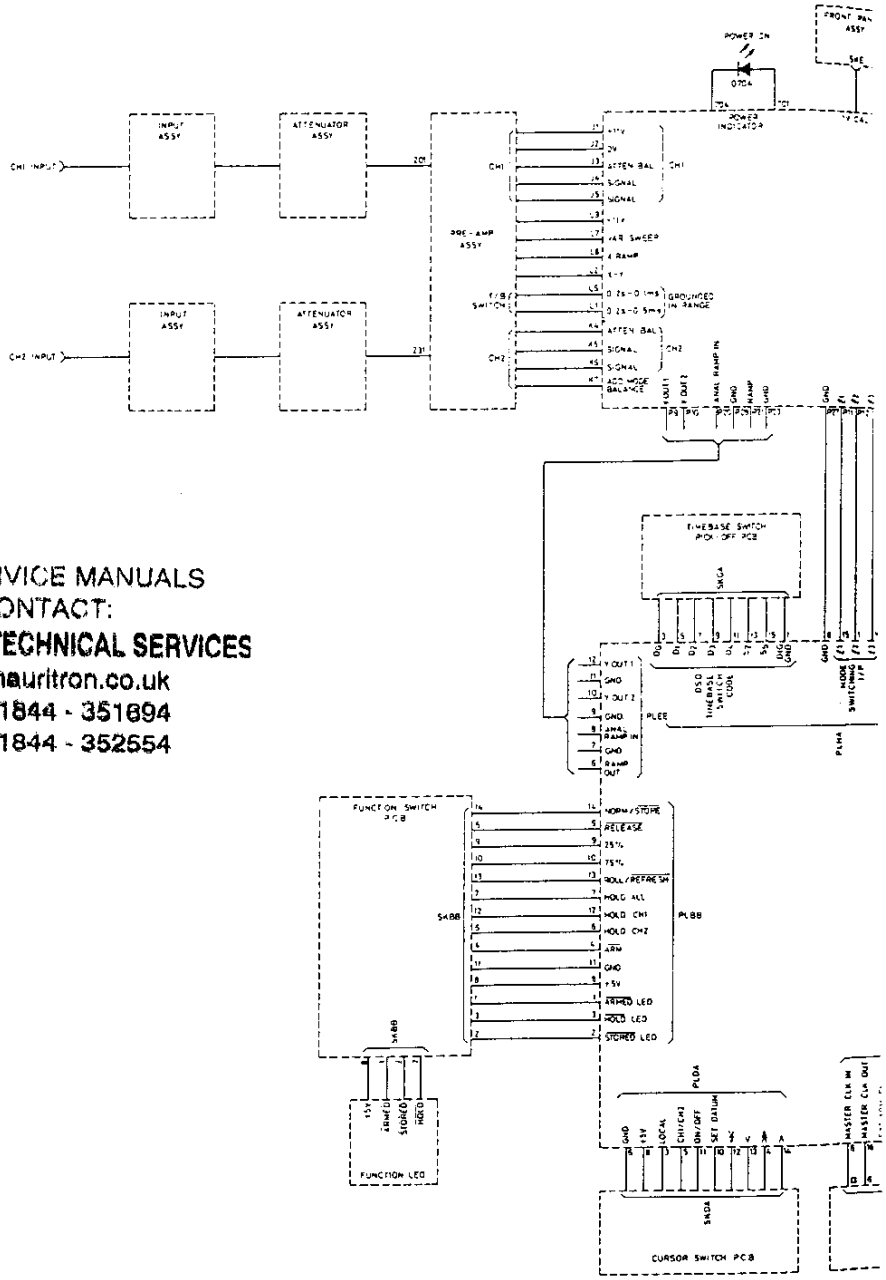
RESISTORS

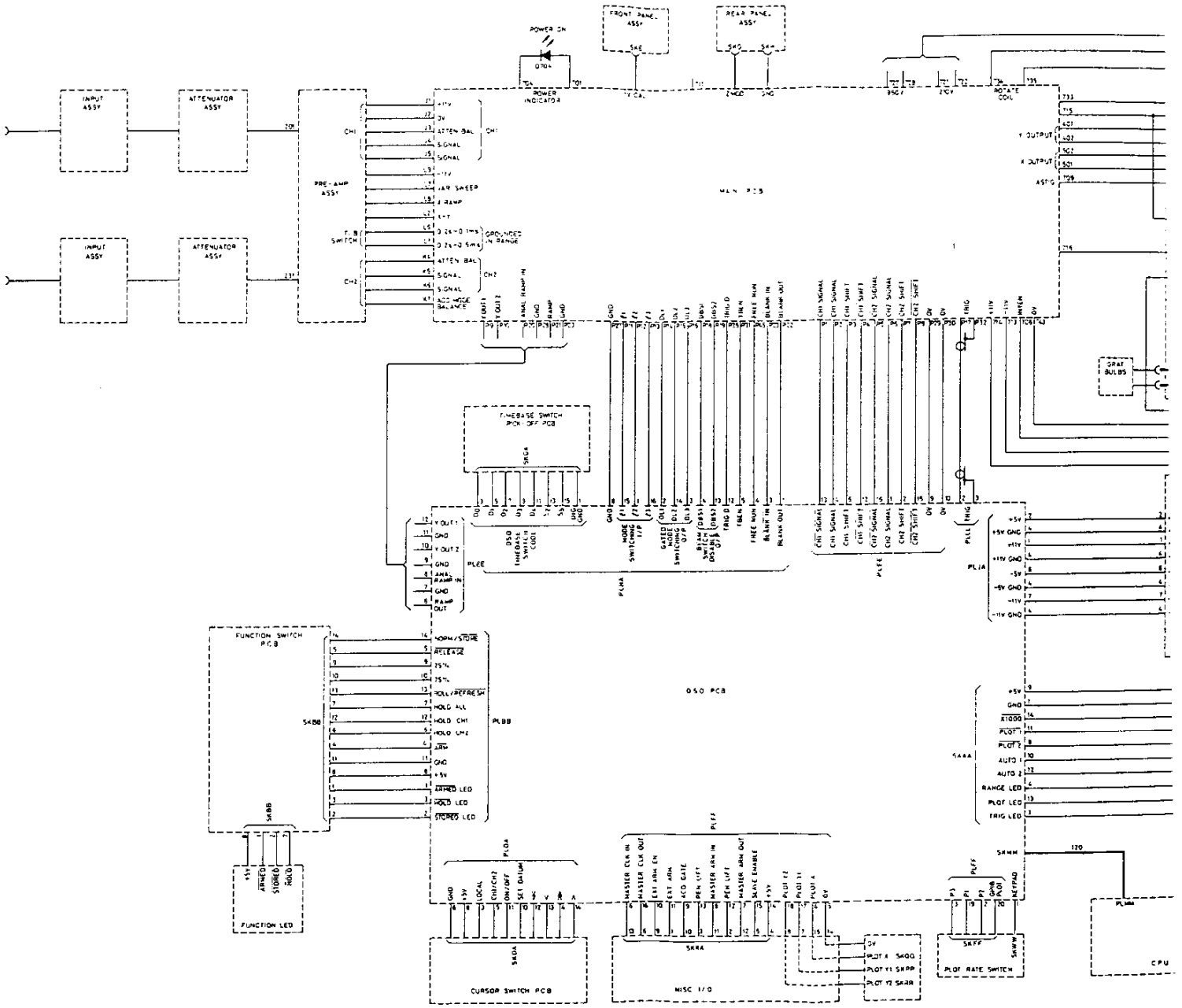
CC	Carbon Composition	½W	10%	unless otherwise stated
CF	Carbon Film	¼W	5%	unless otherwise stated
MO	Metal Oxide	½W	2%	unless otherwise stated
MF	Metal Film	¼W	1%	unless otherwise stated
WW	Wire Wound	6W	5%	unless otherwise stated
CP	Control Potentiometer		20%	unless otherwise stated
PCP	Preset Potenitometer Type MPD, PC		20%	unless otherwise stated
MG	Metal Glaze ½W		5%	unless otherwise stated

CAPACITORS

CE(1)	Ceramic		+80% -25%	
CE(2)	Ceramic	500V	±10%	unless otherwise stated
CE(3)	Ceramic	50V		unless otherwise stated
MF	Metallised Film	100V		unless otherwise stated
SM	Silver Mica			
PF	Plastic Film		±10%	unless otherwise stated
PS	Polystyrene			
PE	Polyester		±10%	unless otherwise stated
PC	Polycarbonate			
E	Electrolytic (Aluminium)		+50% -10%	
T	Tantalum		+50% -10%	

RES	
CAP	
MISC	




POWER ON
D704
POWER INDICATOR
FRONT PANEL ASSY
REAR PANEL ASSY
INPUT ASSY
ATTENUATOR ASSY
PRE-AMP ASSY
MAIN PCB
GRAT BULBS
TIMEBASE SWITCH PICK-OFF PCB
FUNCTION SWITCH P.C.B
FUNCTION LED
CURSOR SWITCH PCB
MISC I/O
PLOT RATE SWITCH
CPU
050 PCB

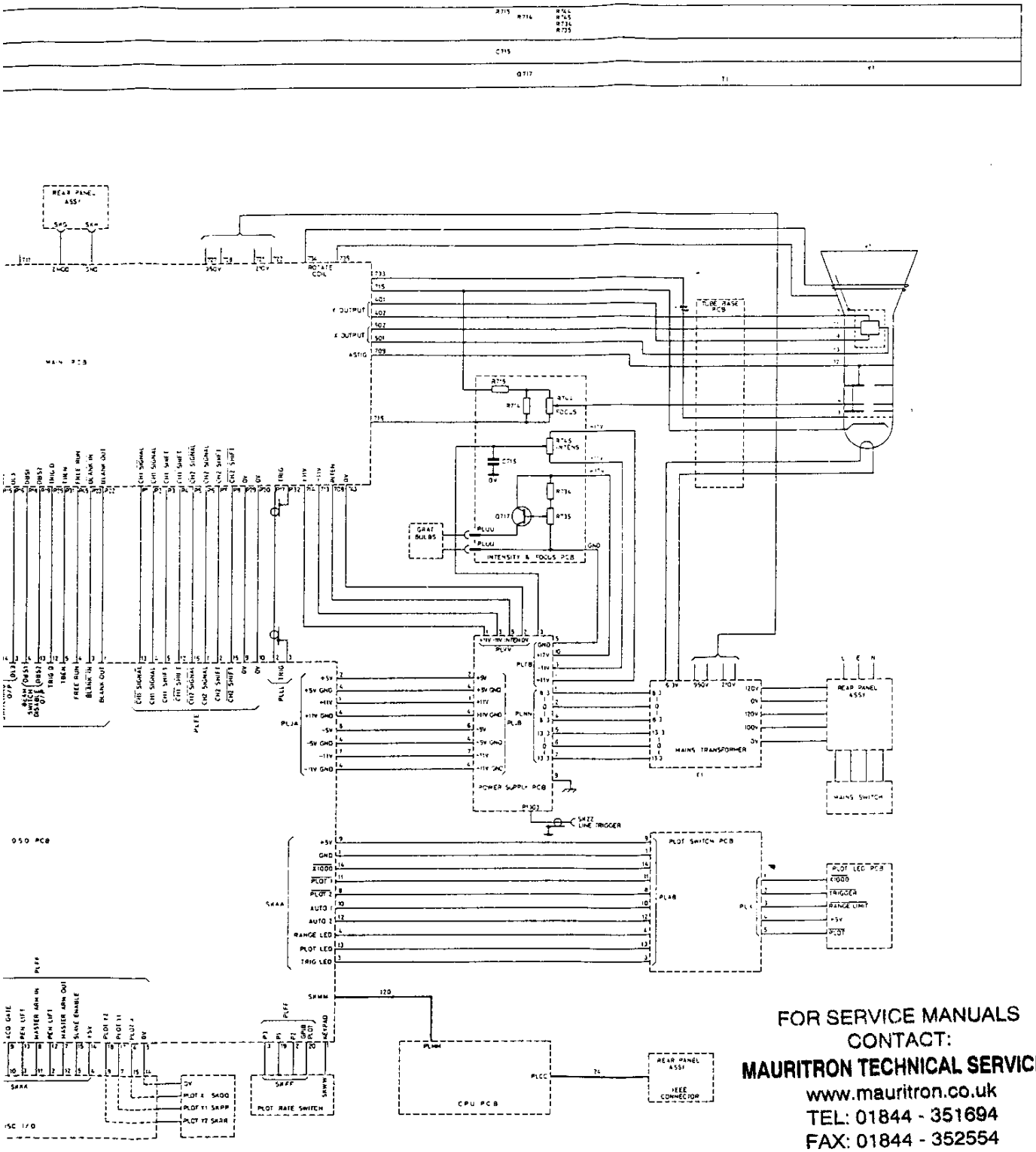
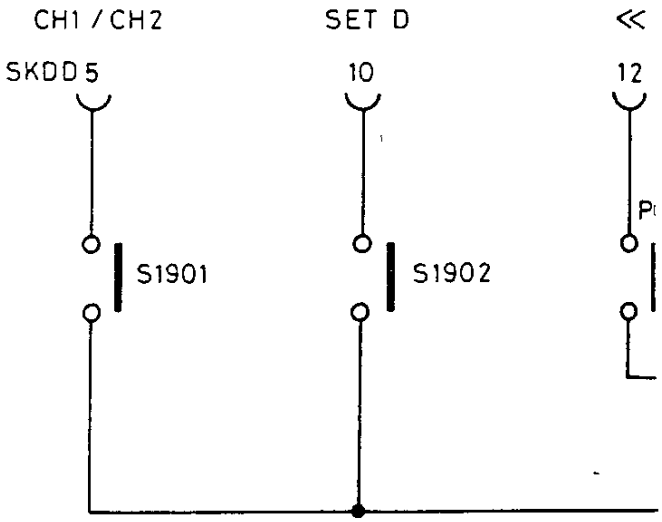


Fig. 18. Interconnection Circuit Diagram

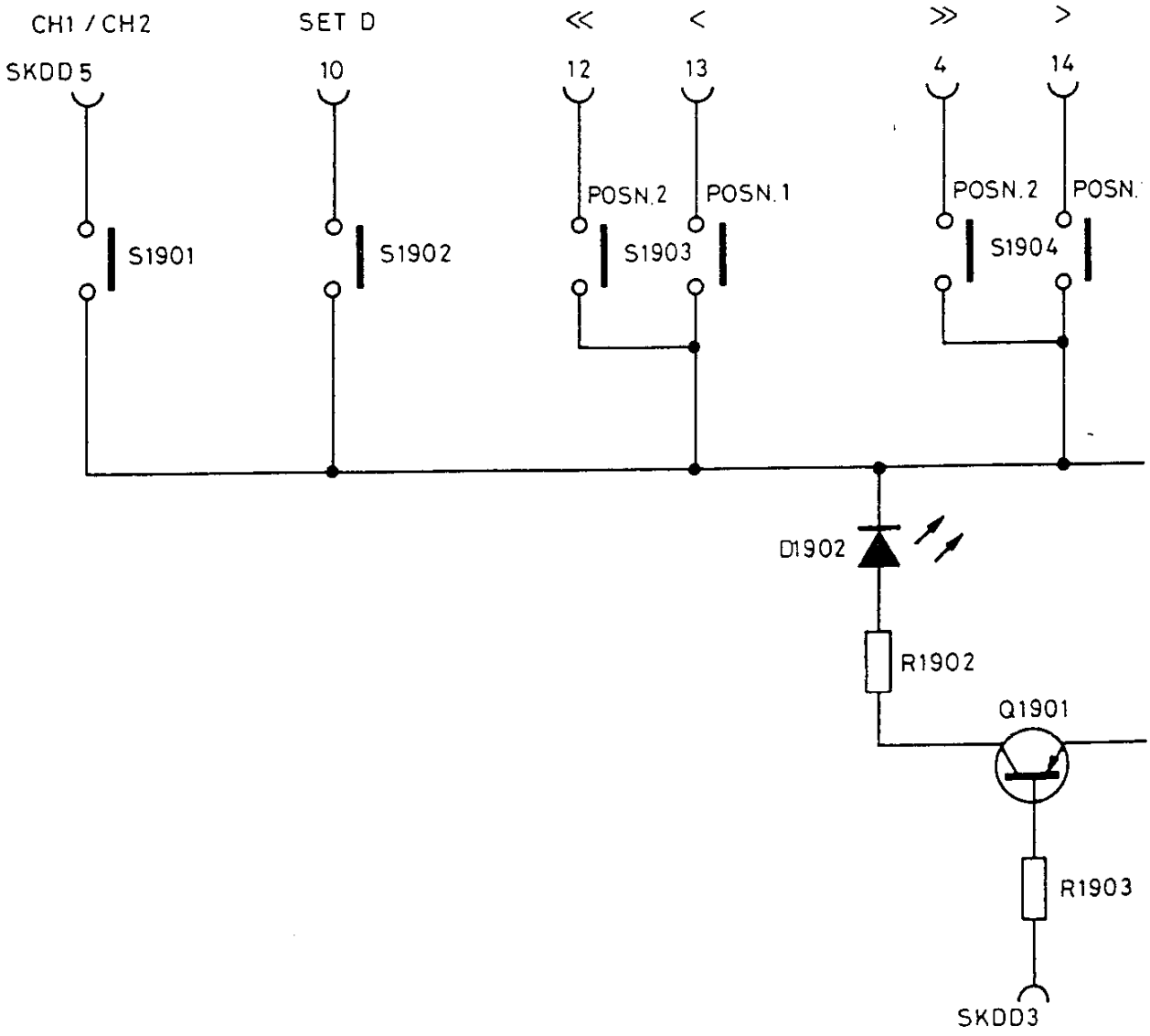
ection 6

Rating	Part No
	43847
	21533
	452880
	452880
	452881
	452881
	452880

RES.	
CAPS.	
MISC.	S1901 S1902 SKDD



S.					R1902	R1903
PS.						
SC.	S1901	S1902	S1903		D1902	S1904
	SKDD					Q1901



	R1902	R1903		R1901
		C1901		
903		S1904	S1905	
	D1902	Q1901		D1901

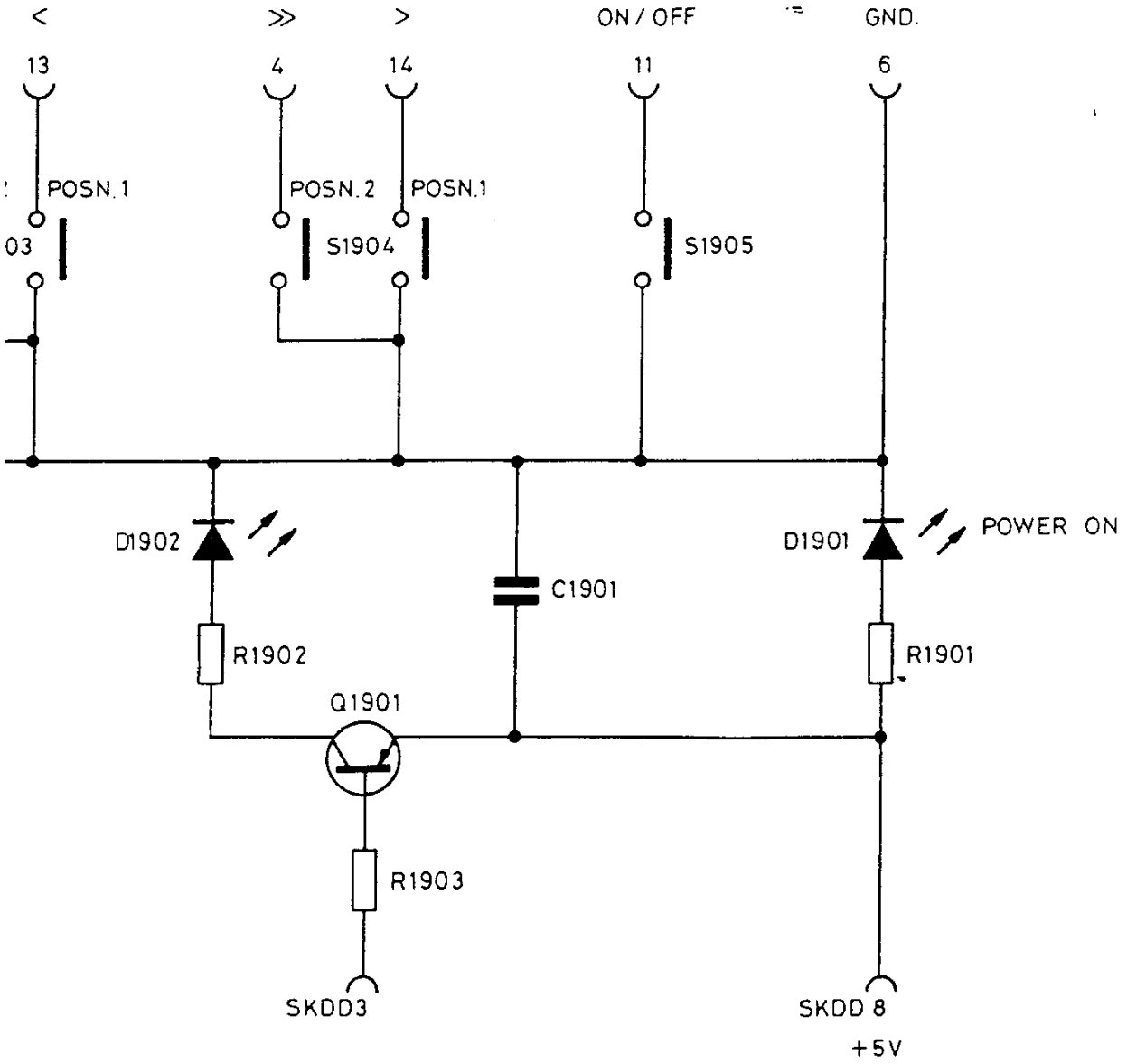


Fig. 19. Cursor Switch Circuit Diagram

CURSOR SWITCH 4035

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R1901	270	CF	5	¼W	28720
R1902	270	CF	5	¼W	28720
R1903	2k7	CF	5	¼W	28726
CAPACITORS					
C1901	10nF	CE(3)		25V	450548
DIODES					
D1901		LED			43847
D1902		LED			43847
Q1901		2N3906			21533
MISCELLANEOUS					
S1901					452880
S1902					452880
S1903					452881
S1904					452881
S1905					452880

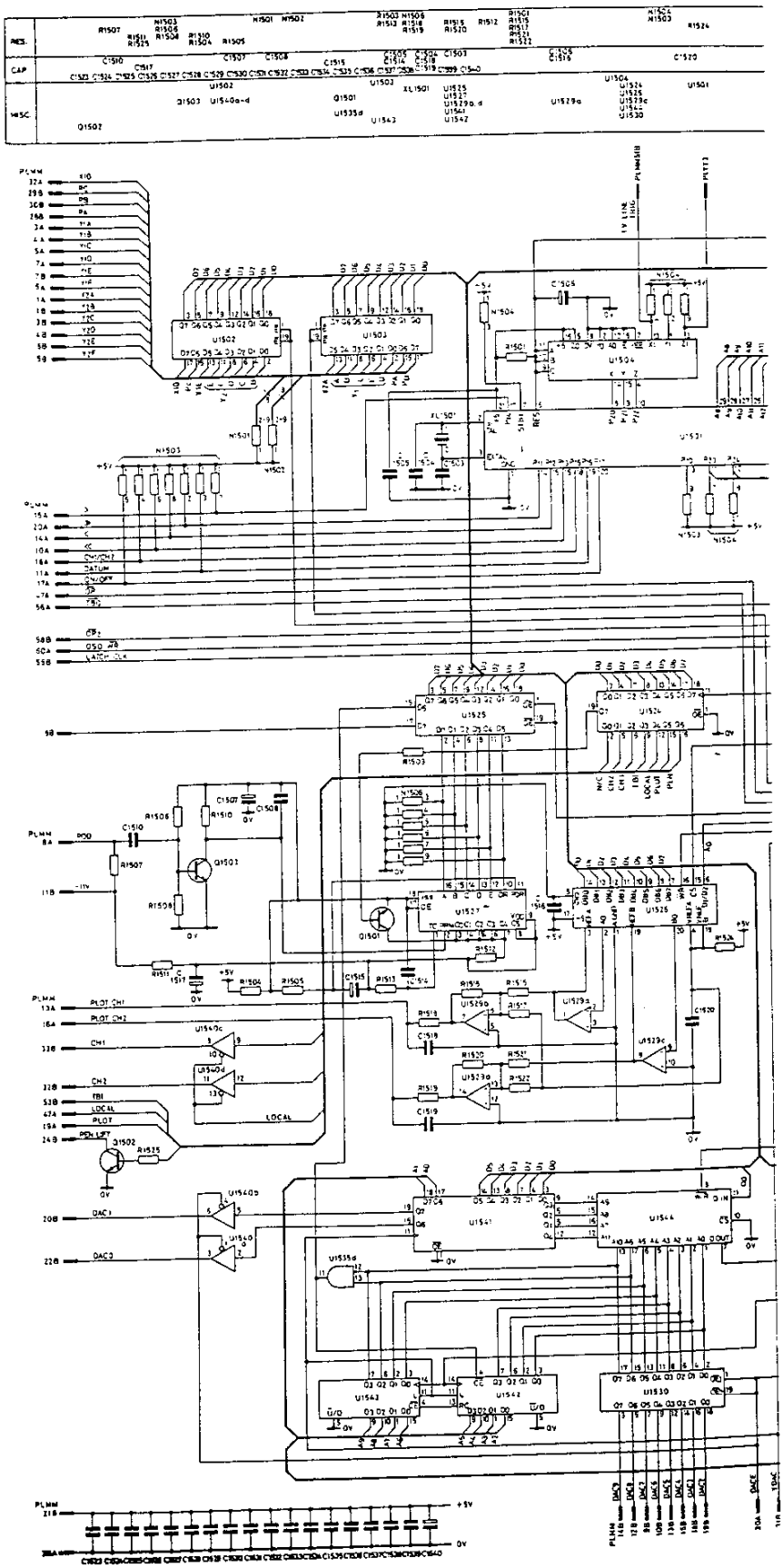
GPIB 4035

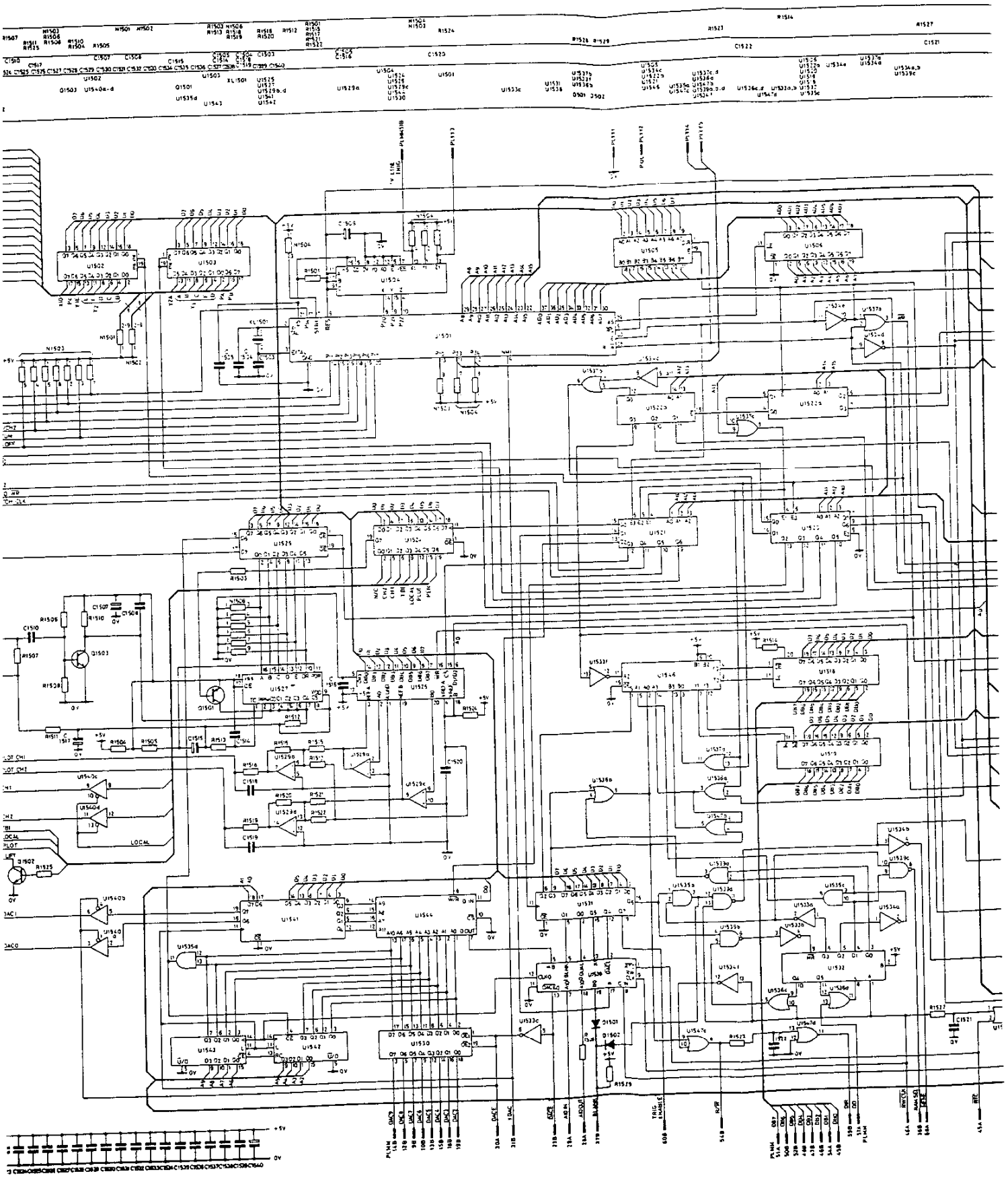
Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
A8	R1501	100k	CF		21819
B7	R1502	4k7	CF		21805
C10	R1503	4k7	CF		21805
E10	R1504	10	CF		21793
E10	R1505	56k	CF		28729
E10	R1506	82k	CF		21818
E10	R1507	100	CF		21794
E10	R1508	22k	CF		21812
E10	R1510	10k	CF		21809
E9	R1511	10	CF		21793
C9	R1512	10k	CF		21809
B10	R1513	56k	CF		28729
E5	R1514	68	CF		28716
C9	R1515	10k	MF	2	38618
C10	R1516	1k8	MF	2	38600
C9	R1517	20k	MF	2	38625
E9	R1518	100	CF		21794
E9	R1519	100	CF		21794
D9	R1520	1k8	MF	2	38600
C9	R1521	10k	MF	2	38618
C10	R1522	20k	MF	2	38625
D2	R1523	10k	CF		21799
C10	R1524	10	CF		21793
E6	R1525	2k2	CF		21802
D1	R1526	3k3	CF		21803
C2	R1527	10k	CF		21809
E6	R1528	100	CF		21794
E5	R1529	4k7	CF		21805
E10	N1501	4k7	Resistor Network		39225
E10	N1502	4k7	Resistor Network		39225
E8	N1503	4k7	Resistor Network		39225
B6	N1504	4k7	Resistor Network		39225
A1	N1505	22k	Resistor Network		35459
B9	N1506	47k	Resistor Network		450602
CAPACITORS					
B2	C1501	10nF	CE(3)	25V	450548
C1	C1502	10nF	CE(3)	25V	450548
A8	C1503	15pF	CE(3)		42410
A8	C1504	15pF	CE(3)		42410
D8	C1505	10nF	CE(3)	25V	450548
B8	C1506	10µF	E	25V	32180
E9	C1507	470nF	CE(3)		43500
E9	C1508	82pF	CE(3)		42419
E10	C1510	220nF	CE(3)		43499
B10	C1514	22nF	MF	100V	39191
B10	C1515	4.7µF	E	63V	32195
C8	C1516	10nF	CE(3)	25V	450548
D9	C1517	220µF	E	16V	32176
E9	C1518	1nF	CE(3)		42432
E9	C1519	1nF	CE(3)		42432

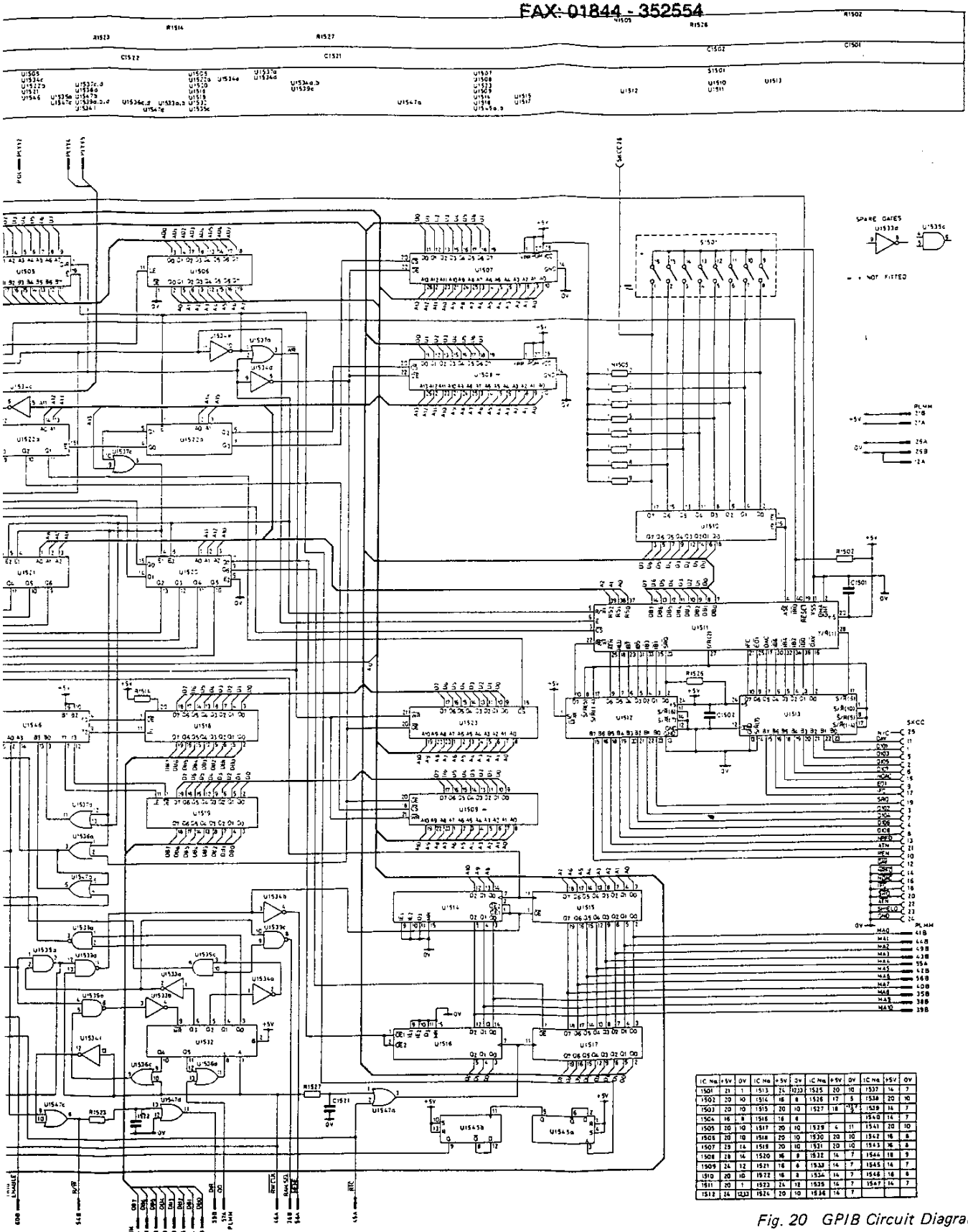
Ref	Value	Description	Tol %±	Rating	Part No
D10	C1520	10nF	CE(3)	25V	450548
D2	C1521	100pF	CE(3)		42420
C2	C1522	100pF	CE(3)		42420
A9	C1523	10nF	CE(3)	25V	450548
A8	C1524	10nF	CE(3)	25V	450548
A5	C1525	10nF	CE(3)	25V	450548
B4	C1526	10nF	CE(3)	25V	450548
A2	C1527	10nF	CE(3)	25V	450548
A1	C1528	10nF	CE(3)	25V	450548
B1	C1529	10nF	CE(3)	25V	450548
C1	C1530	10nF	CE(3)	25V	450548
D1	C1531	10nF	CE(3)	25V	450548
E2	C1532	10nF	CE(3)	25V	450548
D3	C1533	10nF	CE(3)	25V	450548
B3	C1534	10nF	CE(3)	25V	450548
C4	C1535	10nF	CE(3)	25V	450548
E4	C1536	10nF	CE(3)	25V	450548
E5	C1537	10nF	CE(3)	25V	450548
C8	C1538	10nF	CE(3)	25V	450548
B10	C1539	10nF	CE(3)	25V	450548
E9	C1540	22µF	T	35V	35932
C10	Q1501		2N3906		21533
E6	Q1502		2N3904		24146
D9	Q1503		2N3904		24146
DIODES					
E6	D1501		1N4148		23802
E5	D1502		1N4148		23802
INTEGRATED CIRCUITS					
B8	U1501		HD6303		452558
A10	U1502		74C244		450913
A10	U1503		74C244		450913
B6	U1504		4053		41891
A9	U1505		74AlS245		451953
A8	U1506		74HC373		452559
A3	U1507		EPROM 27128		480022
A5	U1508		Not Fitted		
A4	U1509		Not Fitted		
A1	U1510		74C244		450913
B1	U1511		MC68488P		43392
E1	U1512		MC3447		452565
C1	U1513		MC3447		452565
B4	U1514		74HC173		452972
D4	U1515		74HC374		451728
D5	U1516		74C173		452560
E5	U1517		74C374		451266
D6	U1518		74HC373		452559
D4	U1519		74HC373		452559
D3	U1520		74HC138		452561
D3	U1521		74HC138		452561
B4	U1522		74HC139		452562
A4	U1523		2k x 8 Bit Static Ram		450683
D6	U1524		74C374		451266
B9	U1525		74C244		450913

:tion 6

ting	Part No
	44390
	451266
	41092
	41092
	452621
	451290
	451964
	452265
	41476
	450187







IC No.	+5V	0V	IC No.	+5V	0V	IC No.	+5V	0V	IC No.	+5V	0V
1501	21	1	1513	24	12,13	1525	20	10	1537	14	7
1502	20	10	1514	16	8	1526	17	5	1538	20	10
1503	20	10	1515	20	10	1527	18	9	1539	14	7
1504	16	8	1516	16	8				1540	14	7
1505	20	10	1517	20	10	1529	4	11	1541	20	10
1506	20	10	1518	20	10	1530	20	10	1542	16	8
1507	28	14	1519	20	10	1531	20	10	1543	16	8
1508	28	14	1520	16	8	1532	14	7	1544	18	9
1509	24	12	1521	16	8	1533	14	7	1545	14	7
1510	20	10	1522	16	8	1534	14	7	1546	16	8
1511	20	1	1523	24	12	1535	16	7	1547	14	7
1512	24	12,13	1524	20	10	1536	14	7			

Fig. 20 GPIB Circuit Diagram

GPIB 4035 (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
B8	U1526	AD7528			452566
B10	U1527	Not Fitted			
C8	U1529	LF347N			450908
E8	U1530	74C244			450913
D8	U1531	74C374			451266
C3	U1532	74HC164			452563
B5	U1533	74HC04			451958
D2	U1534	74C04			451958
B3	U1535	74HC08			451959
D2	U1536	74HC32			452265
A2	U1537	74HC32			452265
E7	U1538	PAL16R4–4			452622
E2	U1539	74HC00			451956
D5	U1540	74LS125			44390
A7	U1541	74C374			451266
D7	U1542	74LS191			41092
C4	U1543	74LS191			41092
E7	U1544	HM6147–85			452621
E2	U1545	74C74			451290
B4	U1546	74HC157			451964
D2	U1547	74HC32			452265
		MISCELLANEOUS			
A7	XL1501	Crystal 4MHz			41476
A1	S1501	Switch S/P DIL			450187

ANALOGUE BOARD Y AMP 4035

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R1	10	CF			21793
R31	10	CF			21793
R103	22	CF			28710
R110	27	CF		1/8W	43143
R111	120	CF		1/8W	43713
R133	22	CF			28710
R201	180	MF	2		38576
R202	4k7	CF			21805
R203	470	CF			21797
R204	1M	MF			452520
R205	470k	MF			452519
R206	200	MF	2		38577
R207	47	MF	2	1/8W	453447
R208	820	CF		1/8W	44225
R209	240	MF	2	1/8W	453449
R210	56	CF			28715
R211	120	MF	2	1/8W	453448
R212	220	MF	2		38578
R213	4k7	CP			451368
R214	4k7	CF			21805
R215	10k	PCP			453451
R216	100	CF		1/8W	43150
R217	100	CF			21794
R218	220	CF			21796
R219	47	CF		1/8W	43146
R220	2k2	PCP			453450
R231	180	MF	2		38576
R232	4k7	CF			21805
R233	470	CF			21797
R234	1M	MF			452520
R235	470k	MF			452519
R236	200	MF	2		38577
R237	47	MF	2	1/8W	453447
R238	820	CF		1/8W	44225
R239	240	MF	2	1/8W	453449
R240	56	CF			28715
R241	120	MF	2	1/8W	453448
R242	220	MF	2		38578
R243	4k7	CP			451368
R244	4k7	CF			21805
R245	10k	PCP			453451
R246	100	CF		1/8W	43150
R247	100	CF			21794
R248	220	CF	5		21796
R249	47	CF		1/8W	43146
R250	2k2	PCP			453450
R301	10k	PCP			44959
R302	220	PCP			35881
R303	10	CF			21793
R306	1k	CF			21799
R307	10k	PCP			36267
R308	1k	CF			21799
R309	75	CF	2		38567
R311	10	CF			21793
R312	10	CF			21793
R313	100	CF			21794
R314	100	CF			21794
R315	4k7	CP			451371
R316	3k3	MF	2		38606
R317	3k3	MF	2		38606
R318	7k5	CF			40297
R319	7k5	CF			40297
R330	680	MF	2		38590
R331	680	MF	2		38590
R332	47	MF	2		38562
R333	47	MF	2		38562
R334	470	MF	2		38586
R335	470	MF	2		38586
R336	47	MF	2		38562
R337	47	MF	2		38562
R351	10k	PCP			44959
R352	220	PCP			35881
R353	10	CF			21793
R356	1k	CF			21799
R357	10k	PCP			36267
R358	1k	CF			21799
R359	75	MF	2		38567
R361	10	CF			21793
R362	10	CF			21793
R363	100	CF			21794
R364	100	CF			21794
R365	4k7	CP			451371
R366	3k3	MF	2		38606
R367	3k3	MF	2		38606
R368	7k5	CF			40297
R369	7k5	CF			40297
R371	330	CF			28721
R372	330	CF			28721
R380	680	MF	2		38590
R381	680	MF	2		38590
R382	47	MF	2		38562
R383	47	MF	2		38562
R384	470	MF	2		38586
R385	470	MF	2		38586
R386	47	MF	2		38562
R387	47	MF	2		38562
R401	2k2	MF	2		38602
R402	2k2	MF	2		38602

ANALOGUE BOARD Y AMP 4035 (cont.)

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS (cont.)					
R403	2k2	CF			21802
R404	2k2	CF			21802
R405	2k7	MF	2		38604
R406	47	CF			28714
R407	2k7	MF	2		38604
R408	1k5	CF			21801
R409	1k5	CF			21801
R410	1k8	CF			28725
R411	1k8	CF		½W	18553
R412	390	MF	2		38584
R413	1k8	CF		½W	18553
R414	390	MF	2		38584
R415	100	PCP			36958
R416	47	CF			28714
R417	150	MF	2		38574
R418	270	MF	2	½W	26742
R419	10	CF			21793
R421	10	CF			21793
R422	270	MF	2	½W	26742
R423	68	CF			28716
R424	8k2	CF			21808
R425	100	MF	2		38570
R426	160	CF	2		38575
R427	160	CF	2		38575
R428	22	CF			28710
R429	39k	CF		1W	19056
R432	22	CF			28710
R433	47	CF			28714
R434	47	CF			28714
R437	100	CF			21794
R438	100	CF			21794
R439	270	CF		1W	19036
R440	270	CF		1W	19036
R441	270	CF		1W	19036
R442	2k2	MO	5		44986
R443	2k2	MO	5		44986
R444	47	CF			28714
R445	47	CF			28714
R447	47k	CF			21815
R448	47k	PCP			38261
R449	47k	CF			21815
N102		Resistor Network Attenuator			453399
N201		Resistor Network			453400
N202	1k x 5	Resistor Network			453418
N231		Resistor Network			453400
N232	1k x 5	Resistor Network			453418
N301	2k2 x 5	Resistor Network			453419
N351	2k2 x 5	Resistor Network			453419

Ref	Value	Description	Tol %±	Rating	Part No
CAPACITORS					
C102	0.8/pF	Trimmer			451979
C103		Not Fitted			
C104	68pF	CE(2)			22374
C105	100nF	CE(2)		400V	44966
C106	0.8/6pF	Trimmer		500V	451979
C107	0.8/6pF	Trimmer		500V	451979
C108	680pF	CE(2)		160V	40631
C109	0.8/6pF	Trimmer		500V	451979
C133		Not Fitted			
C135	100nF	CE(2)		400V	44966
C201	10nF	CE(3)		25V	450548
C202	2.2nF	CE(2)			22389
C203	10nF	CE(2)		250V	22395
C204	100nF	CE(3)			43498
C205	68pF	CE(3)		A.O.T.	42418
C206	33pF	CE(3)			42414
C207	33pF	CE(2)			36612
C208	10nF	CE(3)		25V	450548
C209	33pF	CE(2)			36612
C211	22pF	CE(3)			42412
C212	1pF	CE(3)			42396
C232	2.2nF	CE(2)			22389
C233	10nF	CE(2)		250V	22395
C234	100nF	CE(3)			43498
C235	68pF	CE(3)		A.O.T.	42418
C236	33pF	CE(3)			42414
C237	33pF	CE(2)			36612
C238	10nF	CE(3)		25V	450548
C239	33pF	CE(2)			36612
C241	22pF	CE(3)			42412
C242	1pF	CE(3)			42396
C269	10nF	CE(3)		25V	450548
C301	10nF	CE(3)		25V	450548
C302	10nF	CE(3)		25V	450548
C303	47pF	CE(3)			42416
C304	4.7μF	CE(3)			53249
C305	100nF	CE(3)			43498
C306	10nF	CE(3)		25V	450548
C351	10nF	CE(3)		25V	450548
C352	10nF	CE(3)		25V	450548
C353	47pF	CE(2)			22372
C354	4.7μF	CE(3)			53249
C356	10nF	CE(3)		25V	450548
C401	10nF	CE(3)			450548
C402	60pF	Trimmer			30286

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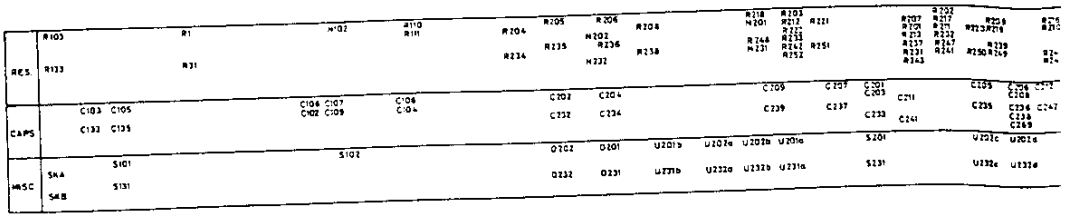
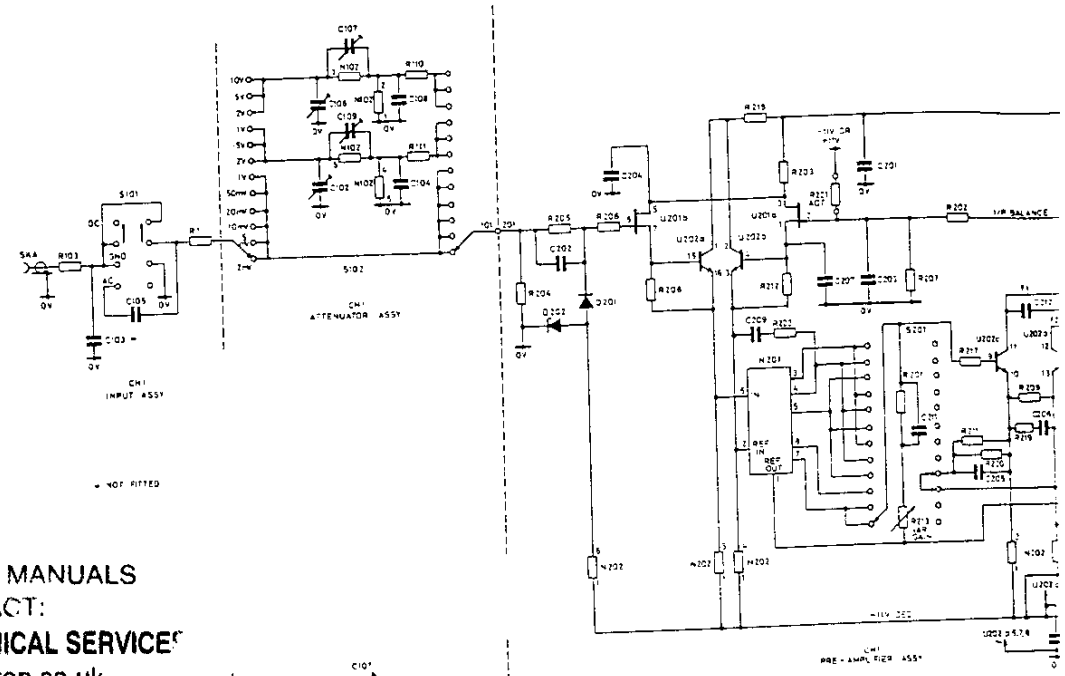
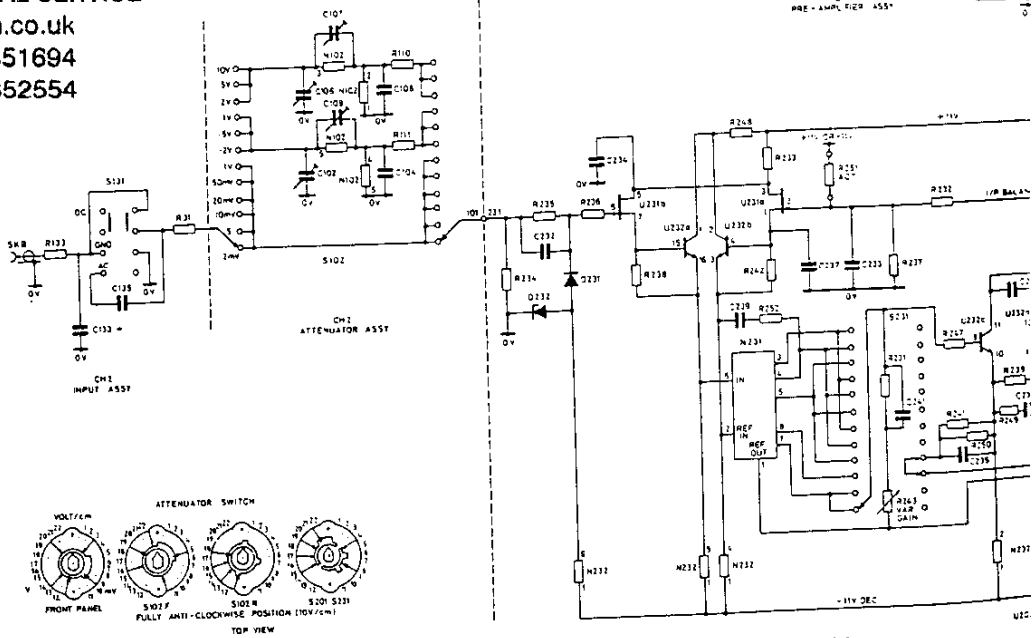
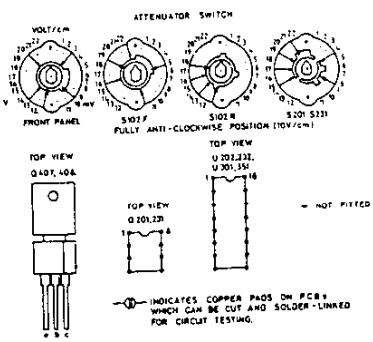
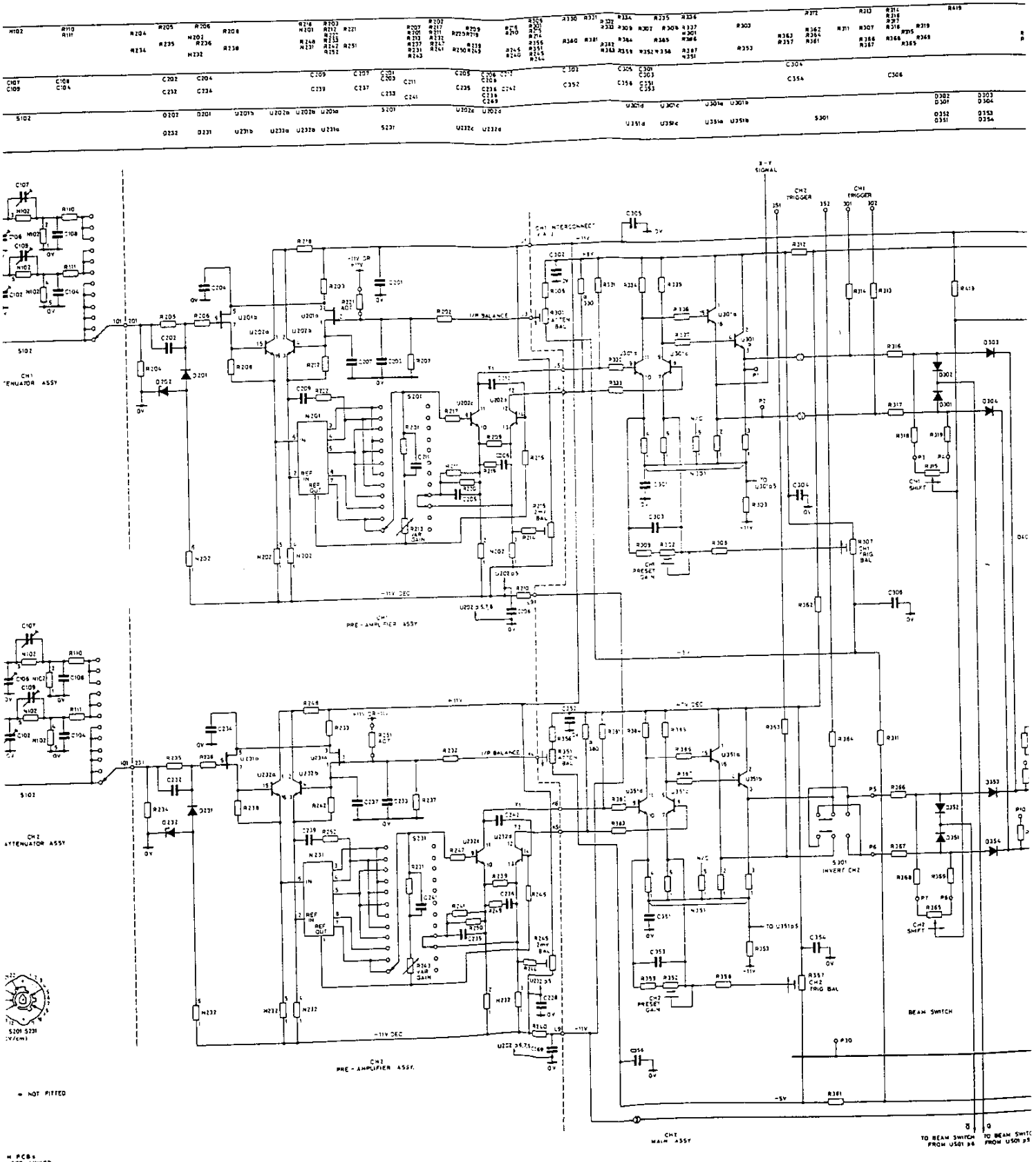
Part No
37401
44993
44993
36275
36275
36275
36275
40788
40788
40056
40056
453170
452279
453170
452280
452280
38729
453414
41046
453414
41046
41046
41046










CH1 ATTENUATOR ASSY
CH1 PRE-AMPLIFIER ASSY
CH2 ATTENUATOR ASSY
CH2 PRE-AMPLIFIER ASSY
CH2 MAIN ASSY
BEAM SWITCH
S301 INVERT CH2
CH1 SHIFT
CH2 SHIFT
CH1 PRESET GAIN
CH2 PRESET GAIN
CH1 TRIG BAL
CH2 TRIG BAL
CH1 ATTEN BAL
CH2 ATTEN BAL
CH1 VAR GAIN
CH2 VAR GAIN
I/P BALANCE
CH1 TRIGGER
CH2 TRIGGER
CH1 INTERCONNECT
TO BEAM SWITCH FROM U501 p6
TO BEAM SWITCH FROM U501 p8
= NOT FITTED
LOER = LINKED

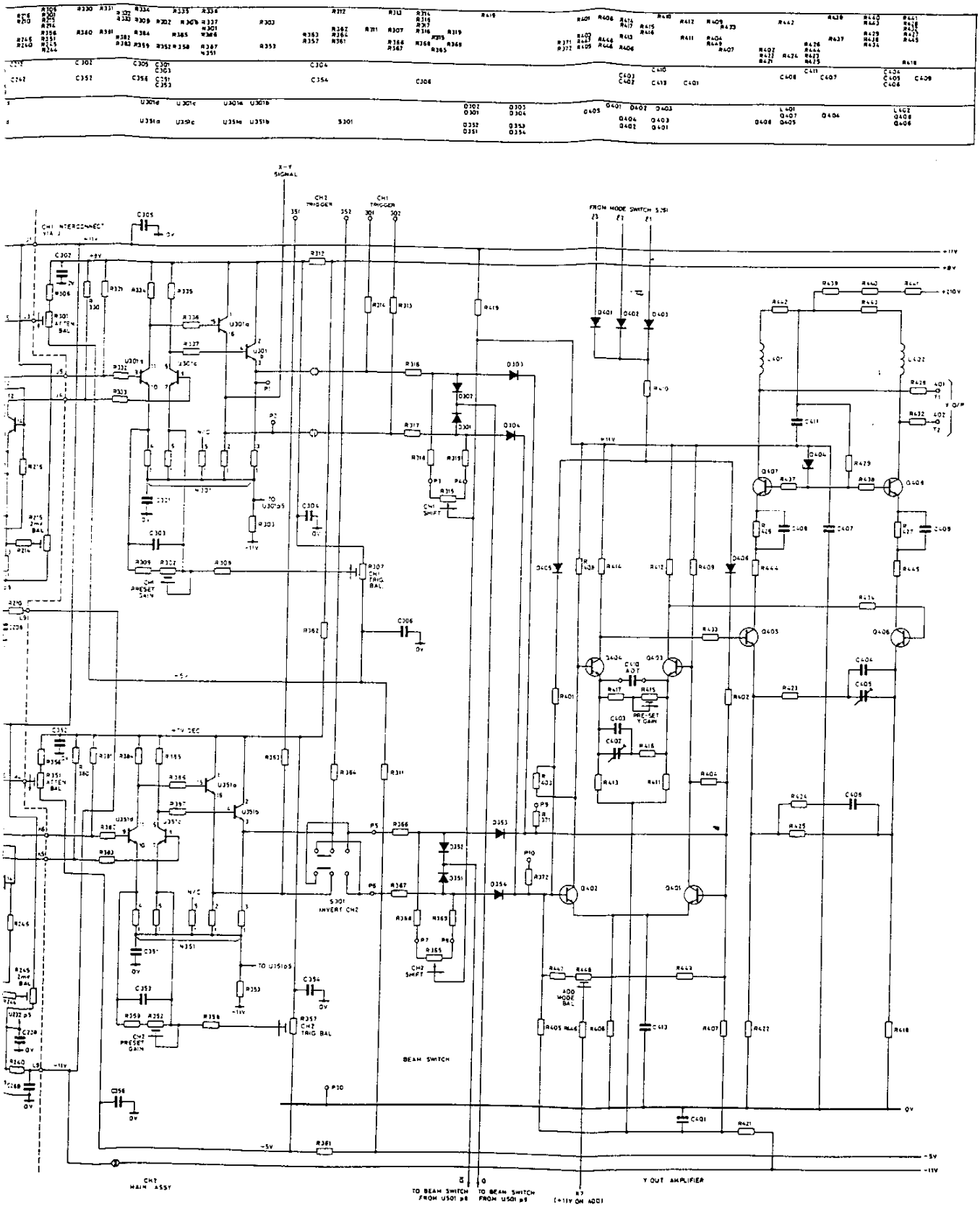


Fig. 21. Y Amp Circuit Diagram

ANALOGUE BOARD Y AMP 4035 (cont.)

Ref	Value	Description	Tol %±	Rating	Part No
CAPACITORS (cont.)					
C403		Not Fitted			
C404	120pF	CE(3)			452156
C405	60pF	Trimmer			30286
C406	39pF	CE(3)			42415
C407	100nF	CE(2)	10%	100V	37018
C408	3.3nF	CE(3)			42438
C409	3.3nF	CE(3)			42438
C410	15pF	CE(3)			42410
C411	5.6nF	CE(2)			22394
C413	1nF	CE(3)			42432
DIODES					
D201		PAD100			453361
D202		ZENER	6V8		33931
D231		PAD100			453361
D232		ZENER	6V8		33931
D301		Schottky Bar 11			452035
D302		Schottky Bar 11			452035
D303		IN4148			34701
D304		IN4148			34701
D351		Schottky Bar 11			452035
D352		Schottky Bar 11			452035
D353		IN4148			34701
D354		IN4148			34701
D401		IN4148			23802
D402		IN4148			23802
D403		IN4148			23802
D404		ZENER			33928
D405		IN4148			34701
D406		IN4148			37401
L401	15µH	Choke	10%		44993
L402	15µH	Choke	10%		44993
TRANSISTORS					
Q401		BF371			36275
Q402		BF371			36275
Q403		BF371			36275
Q404		BF371			36275
Q405		ZTX313			40788
Q406		ZTX313			40788
Q407		BF468			40056
Q408		BF468			40056
MISCELLANEOUS					
S101					453170
S102					452279
S131					453170
S201					452280
S231					452280
S301					38729
U201		Transistor U430			453414
U202		Transistor Array			41046
U231		Transistor U430			453414
U232		Transistor Array			41046
U301		Trans. Array SL3127C			41046
U351		Trans. Array SL3127C			41046

TIMEBASE & TRIGGER 4035

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R151	82K	CF		1W	19060
R261	10	CF			21793
R262	470	CF			21797
R263	4k7	CF			21805
R265	1k	CF			21799
R266	1k	CF			21799
R267	10	CF			21793
R268	100	CF			21794
R269	47k	CP			451367
R270	4k7	CP			451369
R271	2k2	CP			451370
R272	8k2	CF		1/8W	44234
R273	47k	CF		1/8W	44242
R274	2k2	CP			451370
R503	470	CF			21797
R504	56k	CF			28729
R505	27k	CF			21813
R506	10k	PCP			36267
R507	4k7	CF			21805
R508	4k7	CF			21805
R509	33k	CF			21814
R510	10	CF			21793
R511	10k	CF			21809
R512	33k	CF			21814
R513	5k6	CF			21806
R514	1k5	CF			21801
R515	1k5	CF			21801
R516	1k	CF			21799
R517	22k	CF			21812
R518	22k	CF			21812
R519	3k6	MF	2		38607
R520	10k	CF			21809
R521	1k	CF			21799
R522	2k2	CF			21802
R523	4k7	CF			21805
R524	3k9	CF			21804
R525	3k9	CF			21804
R526	2k2	CF			21802
R527	680	CF			28723
R528	680	CF			28723
R529	1k	CF			21799
R530	56	CF			28715
R532	180	CF			21795
R533	1k2	CF			21800
R534	6k8	CF			21807
R535	680	CF			28723
R536	10	CF			21793
R537	10	CF			21793
R538	10	CF			21793
R539	470	CF			21797
R541	1k8	CF			28725
R542	47	CF			28714
R544	470	CF			21797
R545	3k	CF			38605
R546	6k8	CF			21807
R547	2k2	CF			21802
R548	8k2	CF			21808
R549	6k8	CF			21807
R550	4k7	CF			21805
R551	1k	PCP			36264
R552	5k6	CF			21806
R553	4k7	PCP			36266
R554	680	CF			28723
R555	47	CF			28714
R556	2k7	CF			28726
R557	1k8	CF			28725
R558	10	CF			21793
R559	100	CF			21794
R560	68k	CF			21816
R561	100	CF			21794
R562	10k	CF			21809
R563	390	CF		½W	18545
R564	33k	CF			21814
R565	2k2	CF			21802
R566	100k	MF	2	½W	28822
R567	390	CF		½W	18545
R568	22k	CF			21812
R569	510	CF	2		38587
R570	15k	CF			28727
R571	820	CF			28724
R572	22k	CF			21812
R573	4k7	CF			21805
R574	12k	CF		1W	19051
R575	12k	CF		1W	19051
R576	10k	MO	5	¼W	44987
R577	10k	MO	5	¼W	44987
R578	470	CF			21797
R580	47	CF			28714
R600	22k	CF			21812
R601	27k	CF			21813
R603	3k3	CF			21803
R604	4k7	CF			21805
R605	2k2	CF			21802
R606	27k	CF			21813
R607	2k2	CF			21802
R608	4k7	CF			21805
R609	470	CF			21797
R610	10	CF			21793
R611	680	CF			28723
R612	680	CF			28723

TIMEBASE & TRIGGER 4035 (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS (Cont.)					
R613	68k	CF			21816
R614	10	CF			21793
R615	12k	CF			21810
R616	470	CF			21797
R617	2k7	CF			28726
R618	47k	CF			21815
R619	3k3	CF			21803
R620	1M	CF			31840
R621	3k3	CF			21803
R622	1k	CF			21799
R623	150k	CF			21821
R624	10	CF			21793
R626	1M	CF			31840
R627	680	CF			31839
R628	1M	CF			31840
R629	1M	CF			31840
R630	100k	CF			21819
R631	33k	CF			21814
R632	300k	MF	2		38653
R633	18k	CF			21811
R634	6k8	CF			21807
R635	10	CF			21793
R636	68k	CF			21816
R637	4k3	CF	2		38609
R638	3k9	CF			21804
R639	10k	CF			21809
R640	39k	CF			28728
R641	2k2	PCP			36265
R642	56k	CF		1W	19058
R643	470	CF			21797
R644	3k3	CF			21803
R645	10k	CF			21809
R646	2k2	CF			21802
R647	1k5	CF			21801
N261		Resistor Network			38692
CAPACITORS					
C151	10pF	CE(2)			22364
C263	1.2nF	PE		63V	450536
C264	1µF	PE		63V	452523
C265	10nF	CE(2)		25V	450548
C266	4.7µF	T		35V	53249
C267	10nF	CE(2)		25V	450548
C268	10nF	CE(2)		25V	450548
C269	10nF	CE(2)		25V	450548
C270	10nF	CE(2)		25V	450548
C501	22µF	MF		100V	44370
C502	1nF	CE(3)			42432
C503	10nF	CE(2)		25V	450548
C504	10nF	CE(2)		25V	450548
C505	NOT FITTED				
C506	10pF	CE(3)			42408
C507	10nF	CE(2)		25V	450548
C508	10nF	CE(2)		25V	450548
C509	100µF	E		16V	450582
C510	560pF	CE(3)			42429
C511	3.3nF	CE(3)			42438
C512	5.6nF	CE(2)			22394
C513	100µF	E		16V	450582
C514	330pF	CE(3)			452161
C515	150pF	CE(3)			42422
C516	220pF	CE(3)			42424
C517	4.7µF	T			53249
C520	10µF	E		25V	32180
C521	22pF	CE(3)			42412
C522	100nF	CE(3)			43498
C525	10nF	CE(2)		25V	450548
C526	10nF	CE(2)		25V	450548
C601	22nF	CE(2)		250V	39201
C602	100pF	CE(3)			42420
C603	2.2µF	E		63V	32194
C604	2.2µF	E		100V	452245
C605	22pF	CE(2)		50V	42412
C606	100µF	E		16V	450582
C607	100nF	MF		100V	37018
C608	0.22µF	MF		100V	44370
C609	100nF	MF		100V	37018
C610	10nF	CE(2)		25V	450548
C611	22pF	CE(3)			42412
C612	100nF	MF		100V	37018
C613	10nF	CE(2)		25V	450548
C614	47pF	CE(3)			42416
C615	100nF	MF		100V	37018
C616	22µF	CE(2)		25V	32181
C617	47nF	MF		100V	39192
C618	47nF	MF		100V	39192
C619	100pF	CE(3)			42420
C620	10nF	CE(2)		25V	450548
C621	10nF	CE(2)		25V	450548
C622	2.2µF	E		63V	32194
C623	10nF	CE(2)		25V	450548
C624	10nF	CE(2)		25V	450548
C625	10nF	CE(2)		25V	450548
C626	10nF	CE(2)		25V	450548
C627	10nF	CE(2)		25V	450548
C628	10nF	CE(2)		25V	450548
C629	10nF	CE(2)		25V	450548
C630	10nF	CE(2)		25V	450548
C631	10nF	CE(3)		25V	450548
DIODES					
D501		IN4148			23802
D502		0A47			4468
D503		IN4148			23802
D504		IN4148			23802
D505		IN4148			23802

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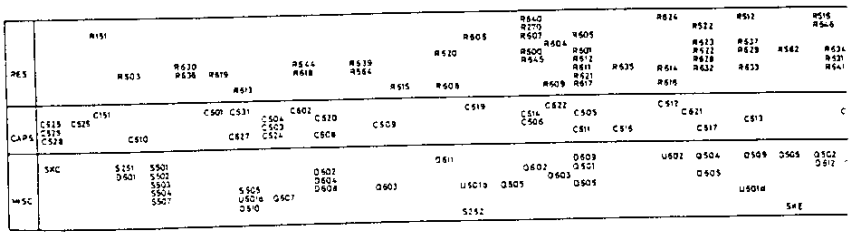
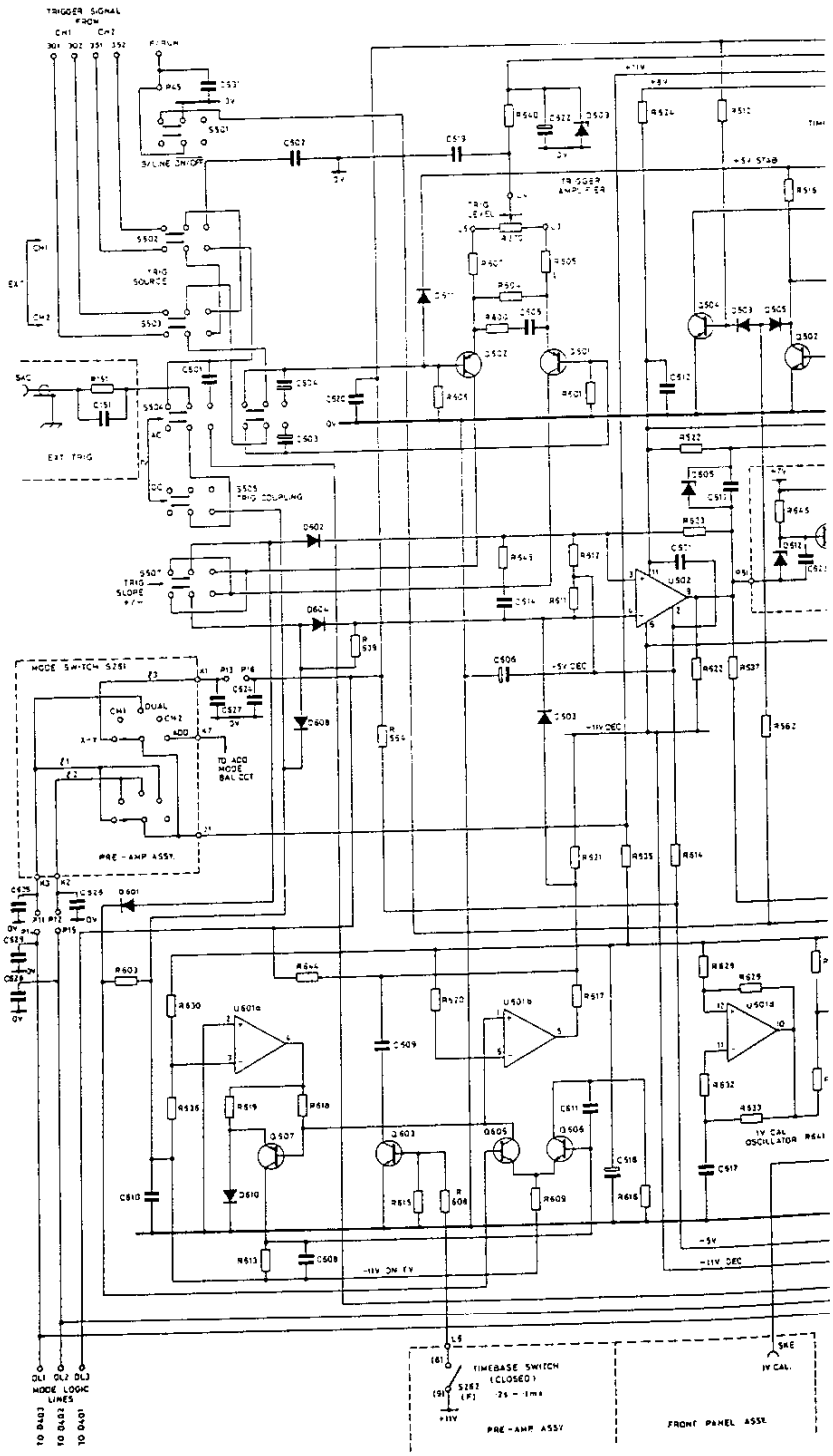
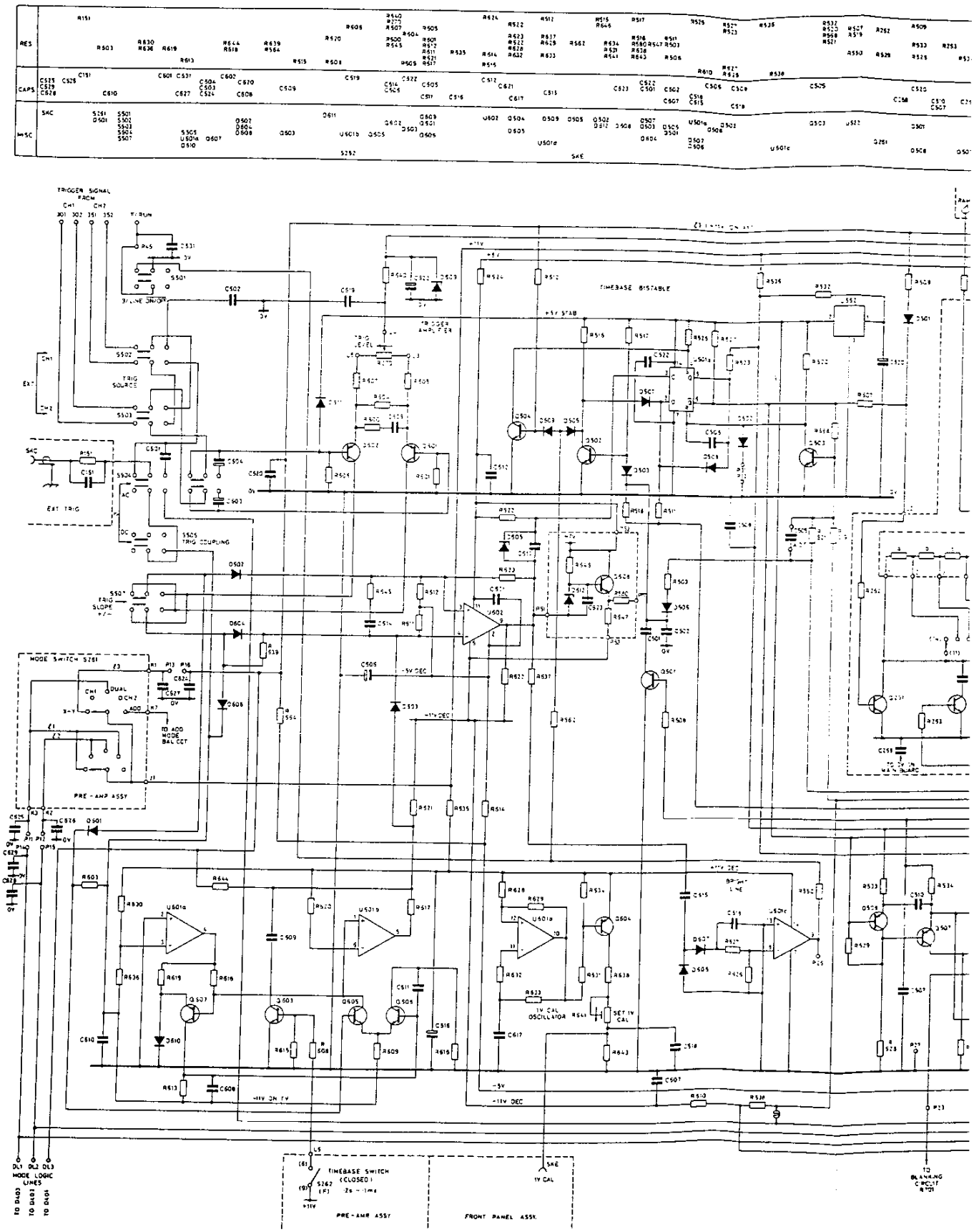
Rating	Part No
	44952
	44950
	44950
	44951
	24146
	21533
	40054
	40054
	450226
	36625
	36625
	44952
	44952
	44951
	44950
	24146
	24146
	21533
	52527
	40130
	36732
	40406
	40061
	40083
	44476
	452249
	38728
	38728
	38728
	38728
	38728
	38728
	38729






TRIGGER SIGNAL FROM
TIMEBASE BISTABLE
TRIGGER AMPLIFIER
TRIG SOURCE
TRIG COUPLING
TRIG SLOPE
EXT TRIG
MODE SWITCH S781
PRE-AMP ASSY
TIMEBASE SWITCH (CLOSED)
1V CAL OSCILLATOR
SET 1V CAL
MODE LOGIC LINES
TO BLANKING CIRCUIT
FRONT PANEL ASSY.

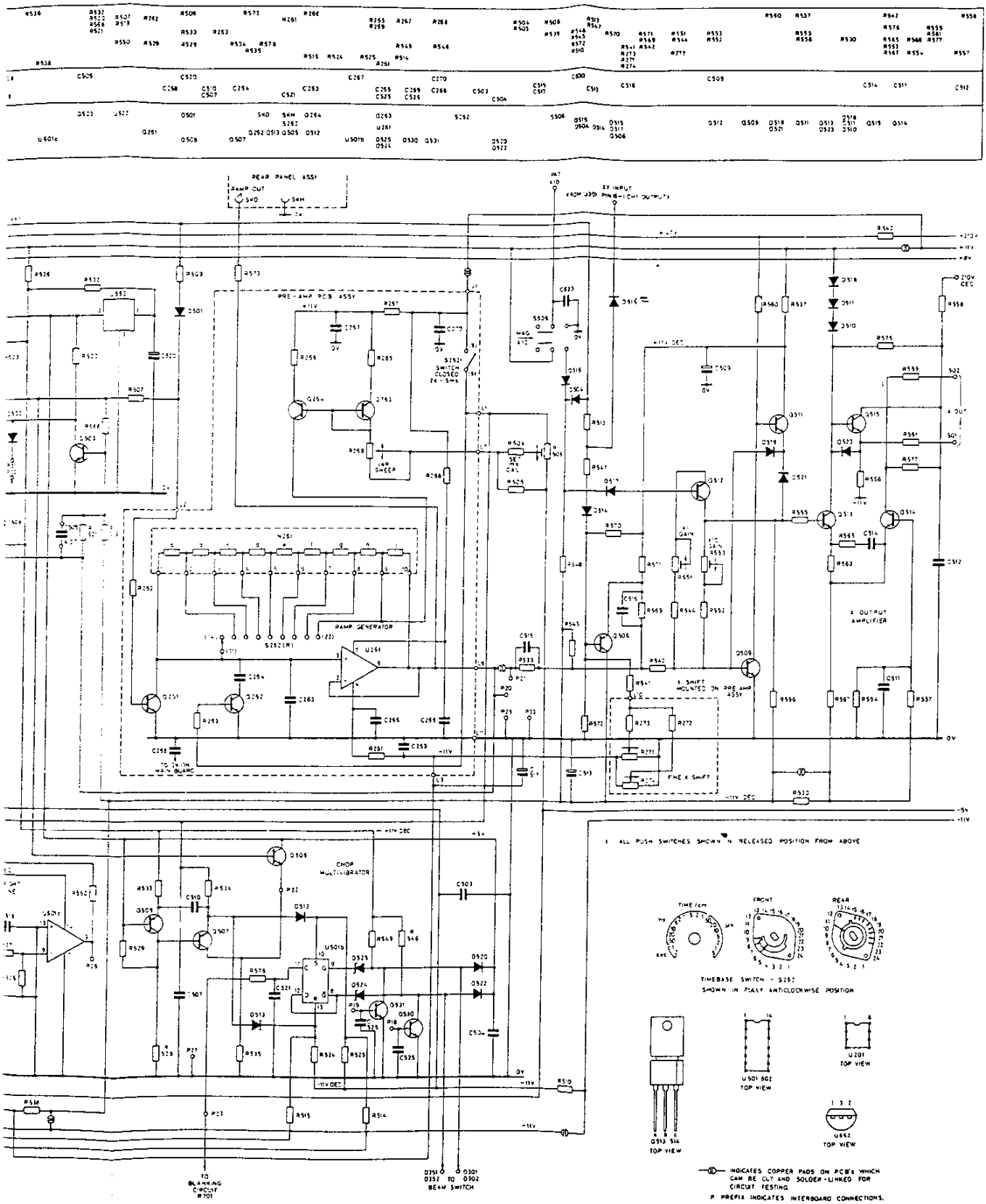


Fig. 22. Timebase Circuit Diagram

TIMEBASE & TRIGGER 4035 (Cont).

Ref	Value	Description	Tol %±	Rating	Part No
DIODES (Cont.)					
D506		IN4148			34701
D507		IN4148			23802
D508		IN4148			23802
D509		IN4148			23802
D510		IN4148			23802
D511		IN4148			23802
D512		IN4148			23802
D513		IN4148			23802
D514		IN4148			23802
D515		IN4148			23802
D516		IN4148			23802
D517		IN4148			23802
D518		IN4148			23802
D519		IN4148			23802
D520		IN4148			23802
D521		ZENER		6V2	33930
D522		IN4148			23802
D523		IN4148			23802
D524		Schottky			452035
D525		Schottky			452035
D601		IN4148			23802
D602		IN4148			23802
D603		IN4148			23802
D604		IN4148			23802
D605		ZENER		5V6	33929
D606		IN4148			23802
D607		IN4148			23802
D608		IN4148			23802
D609		ZENER		47V	40049
D610		IN4148			23802
D611		IN4148			23802
D612				6VZ	33930
TRANSISTORS					
Q261		ZTX313			40788
Q262		BC547B			44951
Q263		BC558C			44952
Q264		BC558C			44952
Q501		BC547B			44951
Q502		MPS2369			36625
Q503		MPS2369			36625
Q504		BC547B			44951
Q505		2N3904			24146

Ref	Value	Description	Tol %±	Rating	Part No
Q506		BC558C			44952
Q507		BC557B			44950
Q508		BC557B			44950
Q509		BC547B			44951
Q511		2N3904			24146
Q512		2N3906			21533
Q513		NSD459			40054
Q514		NSD459			40054
Q515		BF393			450226
Q530		MPS2369			36625
Q531		MPS2369			36625
Q601		BC558C			44952
Q602		BC558C			44952
Q603		BC547B			44951
Q604		BC557B			44950
Q605		2N3904			24146
Q606		2N3904			24146
Q607		2N3906			21533
Q608		TRANS MPS			52527
INTEGRATED CIRCUITS					
U261		LF351N			40130
U501		74LS74			36732
U552		LM78L05			40406
U601		MC3401P			40061
U602		LM710CN			40083
MISCELLANEOUS					
S261					44476
S262					452249
S501					38728
S502					38728
S503					38728
S504					38728
S505					38728
S506					38728
S507					38729

A–D CONVERTER 4035

	Ref	Value	Description	Tol %±	Rating	Part No
	RESISTORS					
M13	R820	10	CF			21793
M13	R821	1k	MF	2		38594
M13	R822	1k	MF	2		38594
L13	R823	470	PCP			36263
M12	R824	150	CF			28719
K13	R825	47	CF			28714
K13	R826	47	CF			28714
L12	R827		A.O.T.			450315
L12	R828	180	CF			21795
K12	R829	240	MF	2		38579
M12	R830	1k2	CF			21800
M12	R831	1k2	CF			21800
L12	R832	180	CF			21795
L12	R833	33	CF			28712
L12	R834	910	MF	2		38593
L12	R835	910	MF	2		38593
L12	R836	1k2	MF	2		38596
K12	R837	750	MF	2		38591
L12	R838	100	CF			21794
M12	R839	10	CF			21793
M12	R840	68	CF			28716
M12	R841	390	CF			28722
L11	R842	330	MF	2		38582
K11	R843	30	MF	2		38557
K11	R844	330	CF			28721
K11	R845	820	CF			28724
M11	R846	22	CF			28710
L11	R847	27	CF			28711
L11	R848	220	CF			21796
L11	R849	360	MF	2		38583
M11	R850	10	CF			21793
M11	R851	47	CF			28714
K12	R852	10	CF			21793
L10	R853	10	CF			21793
M10	R854	220	MF	2		38578
L10	R855	560	CF			21798
L10	R856	220	MF	2		38578
L10	R857	10	CF			21793
M10	R859	1k	CF			21799
M9	R860	22	CF			28710
M9	R861	22	CF			28710
M9	R862	4k7	CF			21805
L9	R863	220	MF	2		38578
M9	R864	10	CF			21793
L9	R865	180	CF			21795
M9	R866	10	CF			21793
M8	R867	100	CF			21794
J8	R868	100	CF			21794
K11	R869	27	CF			28711
K11	R870	47	CF			28714
K13	R873	18k	CF			21811
M13	R874	15k	CF			28727
J12	R875	100k	CF			21819
L10	R876	27	CF			28711
L10	R877	27	CF			28711
L10	R878	100	CF			21794
K13	R879	22k	CF			21812
K13	R880	47k	PCP			38261
M13	R881	220k	CF			21823
L13	R882	100k	PCP			36269
K13	R883	18k	CF			21811
M13	R884	15k	CF			28727
K13	R885	18k	CF			21811
H13	R886	15k	CF			28727
K12	R887	100k	CF			21819
J13	R888	22k	CF			21812
J13	R889	47k	PCP			38261
K13	R890	18k	CF			21811
H13	R891	220k	CF			21823
H13	R892	100k	PCP			36269
H13	R893	15k	CF			28727
H13	R894	100k	CF			21819
H13	R895	10	CF			21793
J13	R896	47	CF			28714
J13	R897	47	CF			28714
H13	R898	1k	MF	2		38594
H12	R901	150	CF			28719
J12	R902		A.O.T.			450315
J12	R903	180	CF			21795
J12	R904	240	MF	2		38579
H12	R905	1k2	CF			21800
H12	R906	1k2	CF			21800
J12	R907	33	CF			28712
J12	R908	910	MF	2		38593
J12	R909	910	MF	2		38593
J12	R910	1k2	MF	2		38596
J12	R911	180	CF			21795
K12	R912	750	MF	2		38591
H12	R913	100	CF			21794
H12	R914	10	CF			21793
H12	R915	68	CF			28716
H12	R916	390	CF			28722
H11	R917	47	CF			28714
J11	R918	330	MF	2		38582
H11	R919	22	CF			28710
H11	R920	27	CF			28711
K11	R921	30	MF	2		38557
K11	R922	330	CF			28721
K11	R923	820	CF			28724
H10	R924	10	CF			21793
J11	R925	220	CF			21796
J11	R926	360	MF	2		38583
H10	R927	10	CF			21793
H10	R928	220	MF	2		38578
H10	R929	560	CF			21798
H10	R930	10	CF			21793

A–D CONVERTER 4035 (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS (Cont.)					
H10	R931	220	MF	2	38578
H9	R932	22	CF		28710
H9	R933	22	CF		28710
J9	R934	220	CF		21796
H9	R935	1k	CF		21799
H9	R936	4k7	CF		21805
H9	R937	47	CF		28714
G9	R938	10	CF		21793
H9	R939	10	CF		21793
J9	R940	180	CF		21795
K9	R941	2k	MF	2	38601
K9	R942	4k3	MF	2	38609
J9	R943	16	MF	2	38551
J10	R948	27	CF		28711
J10	R949	27	CF		28711
J10	R950	820	CF		28724
J10	R951	820	CF		28724
K10	R952	82	CF		28717
J10	R953	100	CF		21794
K12	R954	10	CF		21793
K11	R955	27	CF		28711
K11	R956	47	CF		28714
J8	R957	47	CF		28714
H9	R964	10	CF		21793
L10	R965	10	CF		21793
M9	R966	47	CF		28714
L10	R967	820	CF		28724
L10	R968	820	CF		28724
M13	R969	100k	CF		21819
K8	R970	100	CF		21794
M11	R971	47	CF		28714
M9	R972	47	CF		28714
H9	R973	47	CF		28714
H11	R974	47	CF		28714
K9	R975		A.O.T.		
K10	R976	82	CF		28717
K12	R1055	10	CF		21793
K12	R1056	10	CF		21793
K8	N808	330 x 8	Resistor Network		44880
K9	N809	330 x 8	Resistor Network		44880
CAPACITORS					
K12	C802	10pF	CE(3)		42408
K12	C803	10pF	CE(3)		42408
H12	C804	10pF	CE(3)		42408
J13	C805	10pF	CE(3)		42408
	C808	82pF			42419
H12	C840	10nF	CE(3)	25V	450548
L12	C841		A.O.T.		
L12	C842	10nF	CE(3)	25V	450548
L12	C843	15pF	CE(3)		42410
	C844	10nF	CE(3)	25V	450548
	C845	5.6pF	CE(3)		42405
	C846	10nF	CE(3)	25V	450548
	C847		A.O.T.		
	C848	10nF	CE(3)	25V	450548
	C849	10nF	CE(3)	25V	450548
	C850	10nF	CE(3)	25V	450548
	C851	39pF	CE(3)		42415
	C852	10pF	CE(3)		42408
	C853	10nF	CE(3)	25V	450548
	C854	10nF	CE(3)	25V	450548
	C855	1nF	CE(3)		42432
	C856	1nF	CE(3)		42432
	C857	10nF	CE(3)	25V	450548
	C858	10nF	CE(3)	25V	450548
	C859	10nF	CE(3)	25V	450548
	C860	39pF	CE(3)		42415
	C861	56pF	CE(3)		42417
	C862	10nF	CE(3)	25V	450548
	C863	10nF	CE(3)	25V	450548
	C864	10nF	CE(3)	25V	450548
	C865	1µF	T	35V	34895
	C866	1µF	T	35V	34895
	C867	10nF	CE(3)	25V	450548
	C868	10nF	CE(3)	25V	450548
	C869	10nF	CE(3)	25V	450548
	C870	10nF	CE(3)	25V	450548
	C871	10nF	CE(3)	25V	450548
	C872	10nF	CE(3)	25V	450548
	C874	100nF	CE(3)		43498
	C875	100nF	CE(3)		43498
H13	C876	10nF	CE(3)	25V	450548
J12	C877		A.O.T.		
H12	C878	10nF	CE(3)	25V	450548
H12	C879	15pF	CE(3)		42410
J12	C880	10nF	CE(3)	25V	450548
H12	C881	5.6pF	CE(3)		42405
H11	C882	10nF	CE(3)	25V	450548
H11	C883	5.6pF	CE(3)		42405
H12	C884	10nF	CE(3)	25V	450548
K11	C885	10nF	CE(3)	25V	450548
H11	C886		A.O.T.		
H10	C887	1nF	CE(3)		42432
H10	C888	1nF	CE(3)		42432
H11	C889	39pF	CE(3)		42415
H10	C890	10pF	CE(3)		42408
J11	C891	10nF	CE(3)	25V	450548
H10	C892	10nF	CE(3)	25V	450548
H10	C893	10nF	CE(3)	25V	450548
J9	C894	10nF	CE(3)	25V	450548
G9	C895	10nF	CE(3)	25V	450548
K11	C896	10nF	CE(3)	25V	450548
H10	C897	10nF	CE(3)	25V	450548
J9	C898	22µF	E	16V	450580

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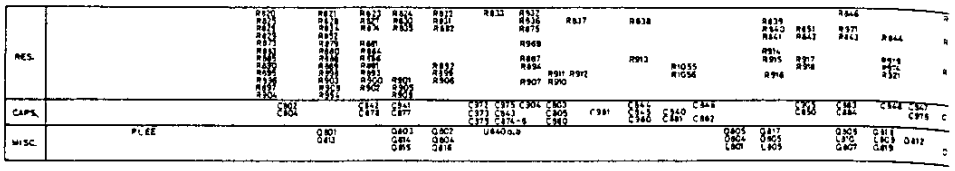
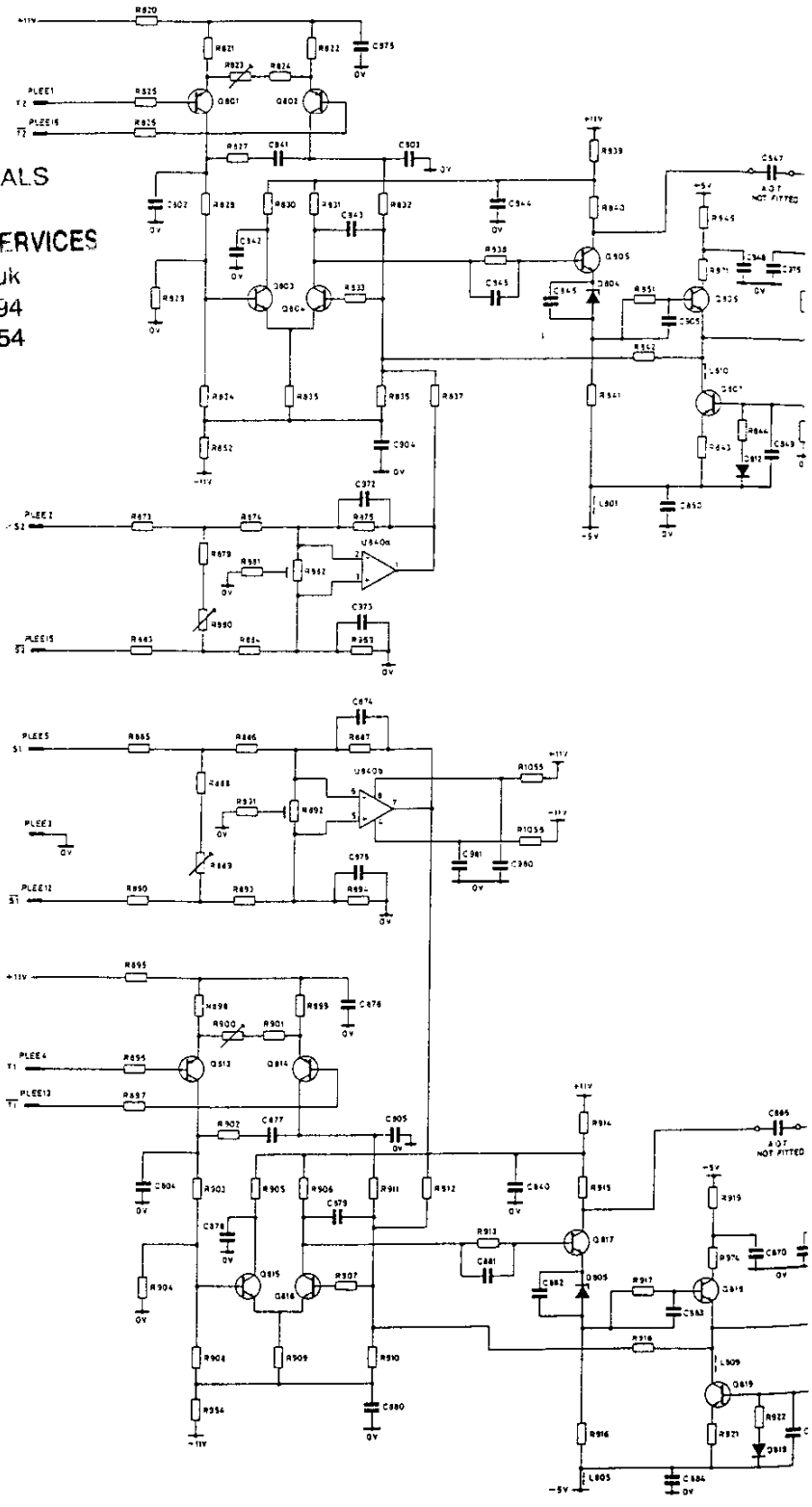
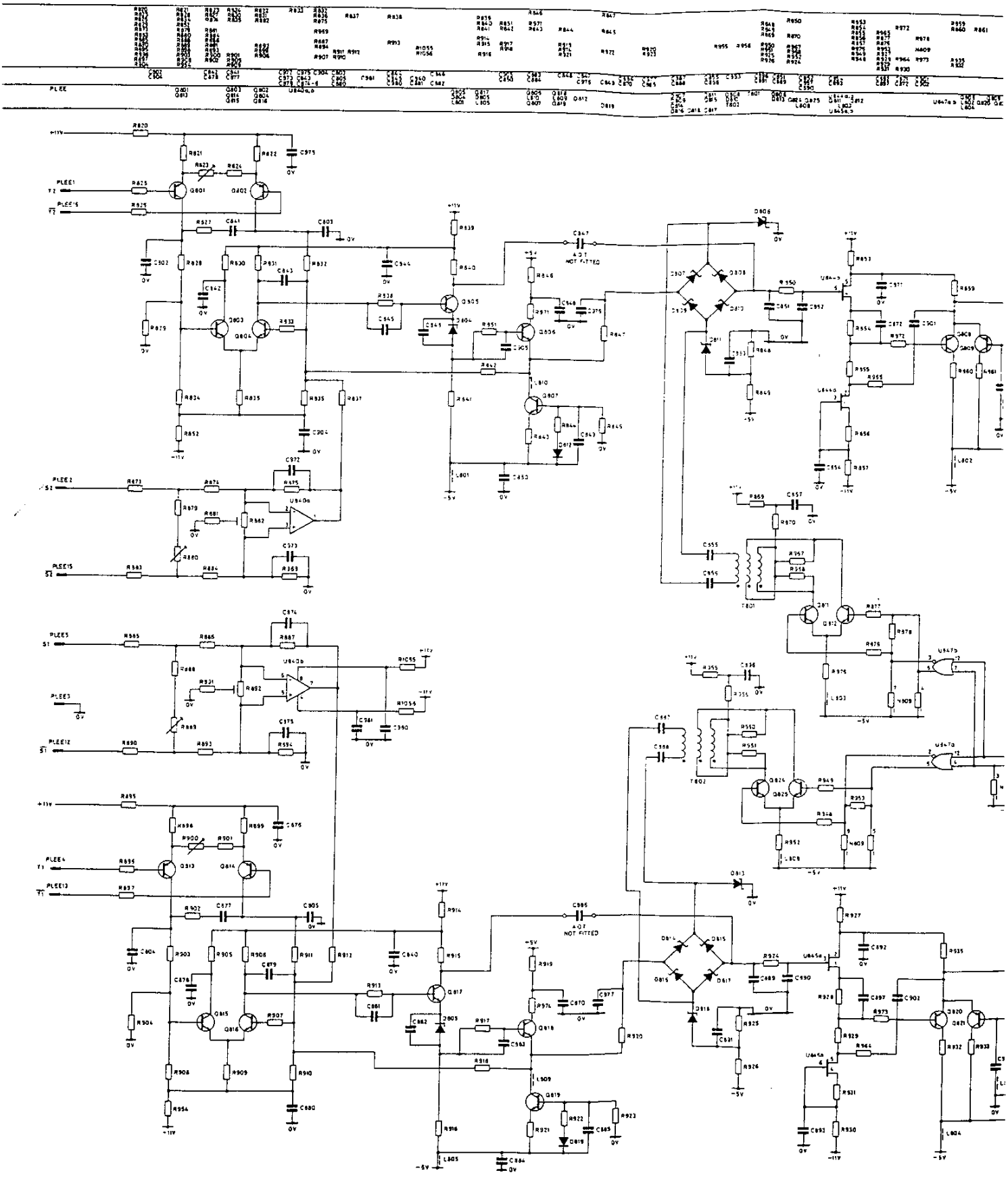
±%	Rating	Part No
		452760
		452760
		452760
		452760
		452760
		452760
		452760
		452760
		452760
		452760
		452760
		452760
		452271
		452271
		24128
		24128
		36625
		36625
		36625
		39019
		23307
		24128
		24128
		39271
		39019
		39019
		24128
		24128
		36625
		36625
		36625
		39019
		23307
		24128
		24128
		39271
		24128
		39019
		39019
		451262
		40130
		451946
		451946
		450919
		450919
		39903
		451809







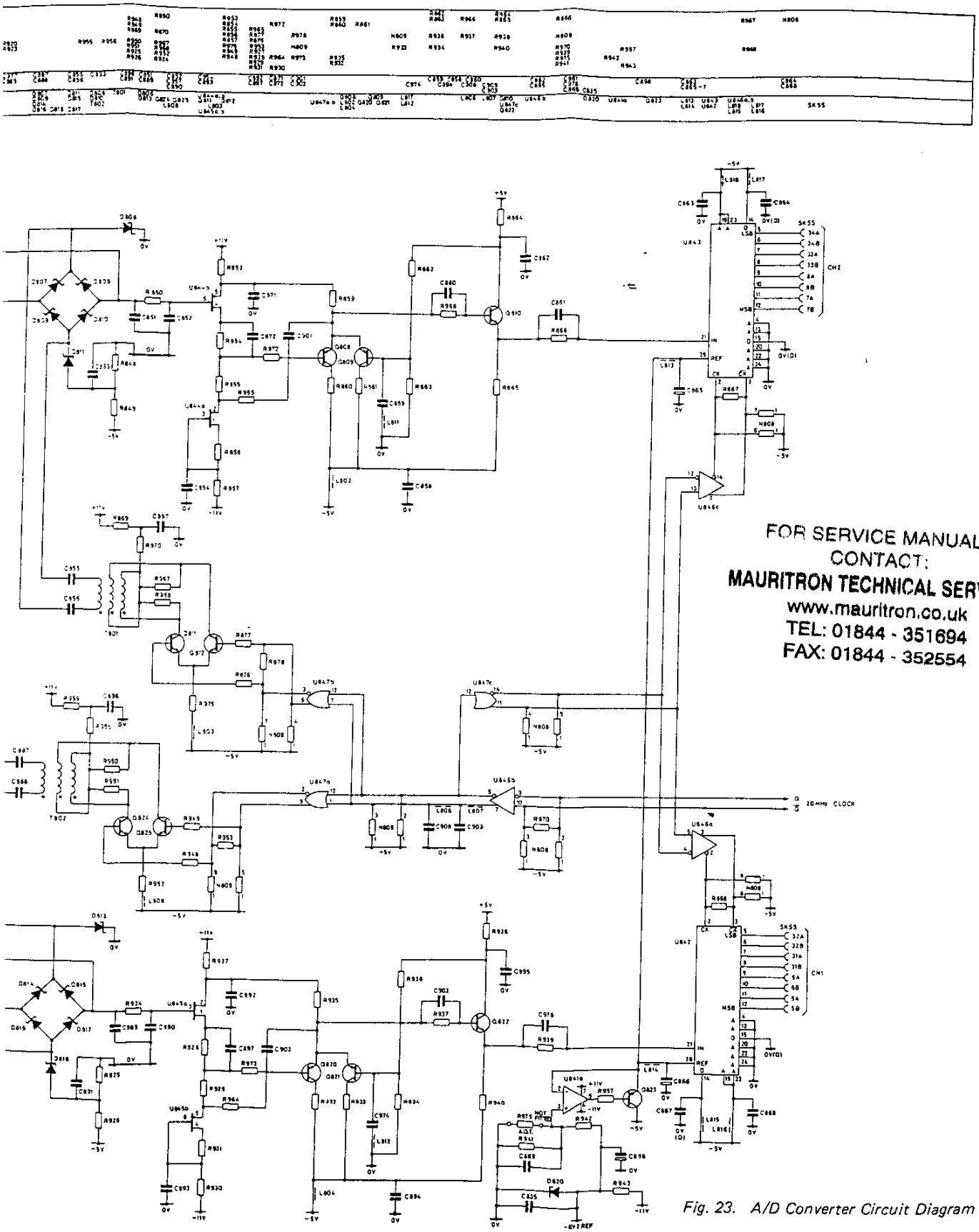


Fig. 23. A/D Converter Circuit Diagram

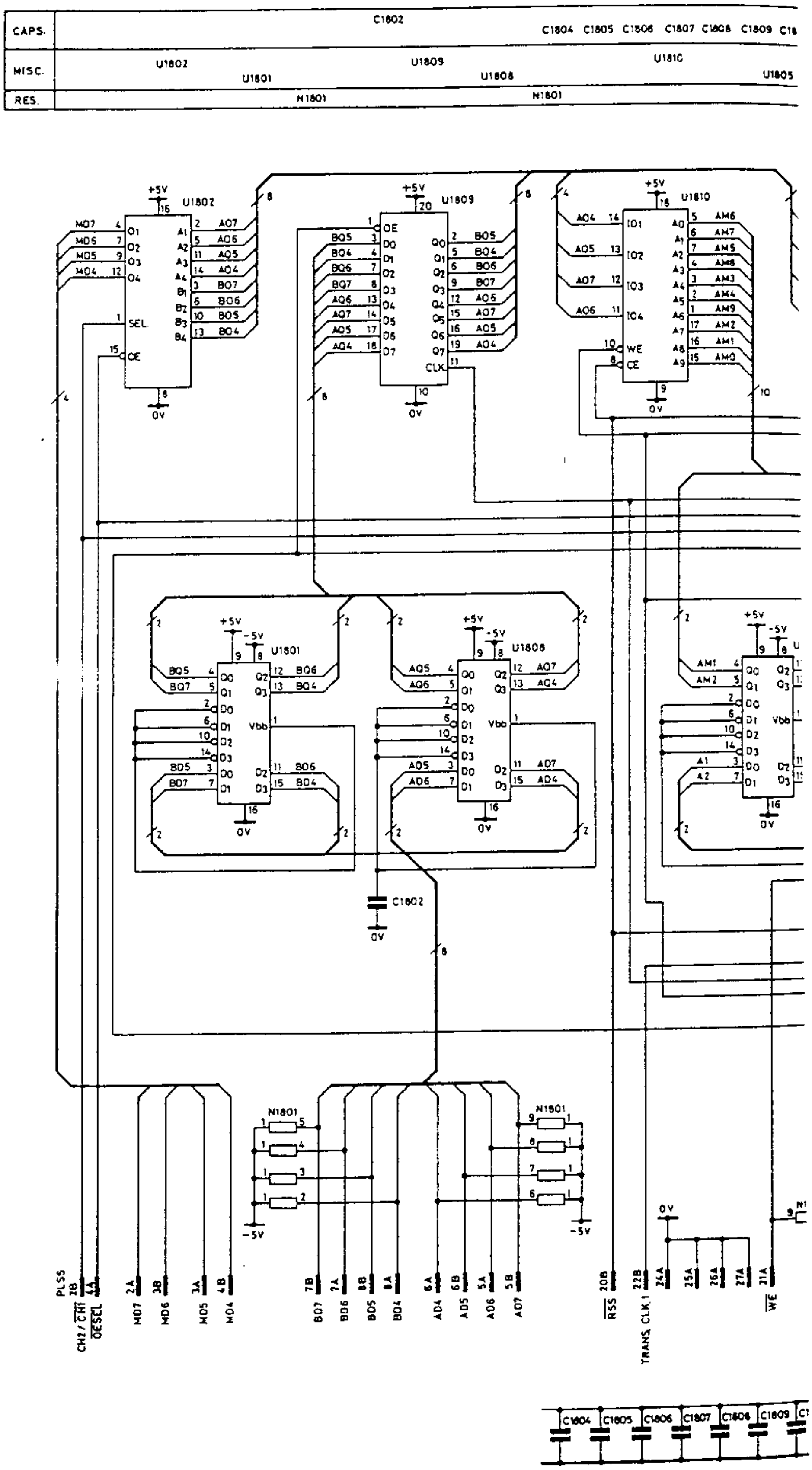
A–D CONVERTER 4035 (Cont.)

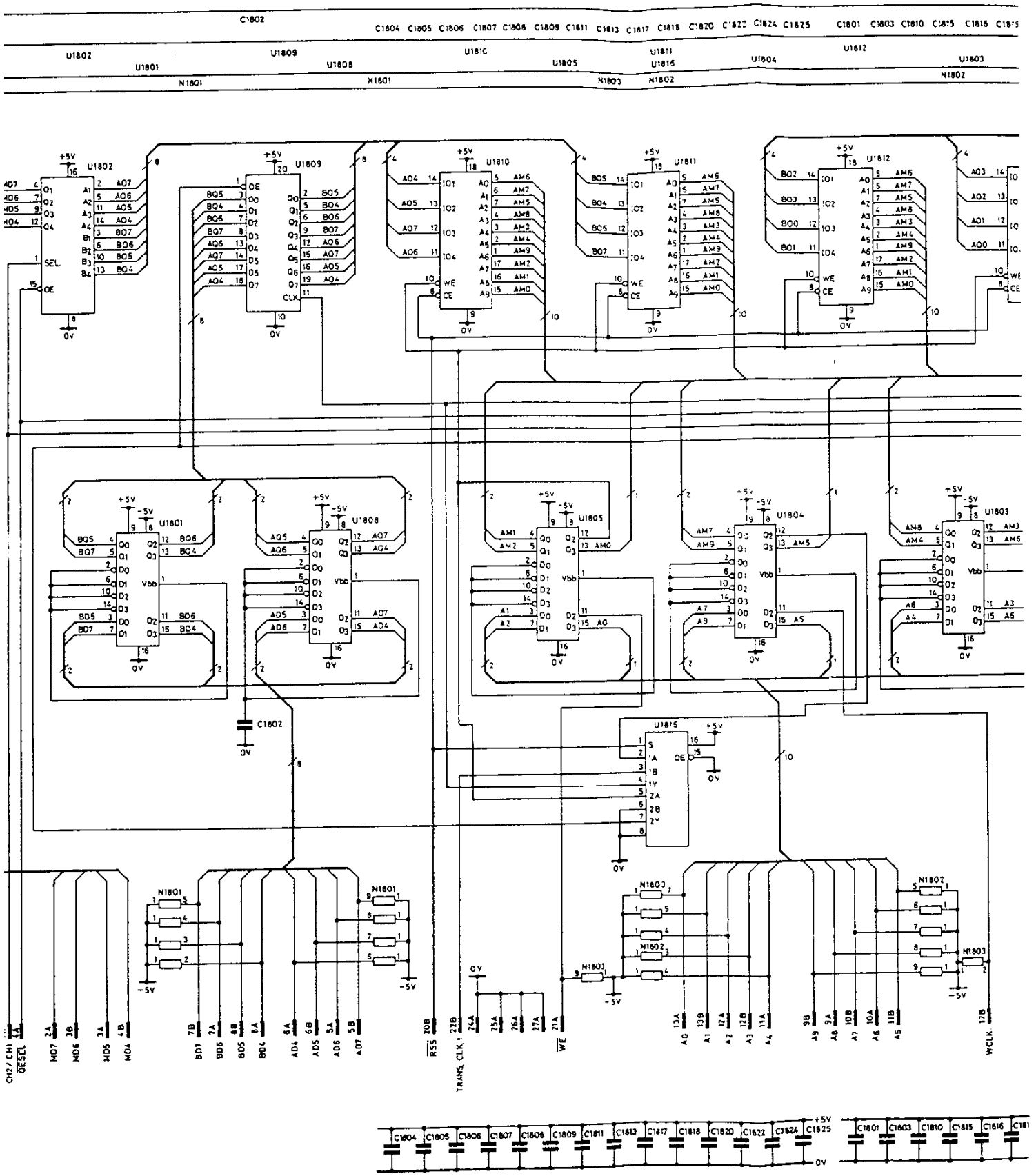
	Ref	Value	Description	Tol %±	Rating	Part No
	CAPACITORS (Cont.)					
	C899	100nF	CE(3)			43498
	C900	100nF	CE(3)			43498
M9	C901	560pF	CE(3)			42429
H9	C902	560pF	CE(3)			42429
H9	C903	39pF	CE(3)			42415
K12	C904	10nF	CE(3)		25V	450548
L11	C905	5.6pF	CE(3)			42405
K9	C908	18pF	CE(3)			42411
L9	C909	22pF	CE(3)			42412
E13	C945	10nF	CE(3)		25V	450548
K5	C946	10nF	CE(3)		25V	450548
J12	C972	100nF	CE(3)			43498
M13	C973	100nF	CE(3)			43498
J9	C974	10nF	CE(3)		25V	450548
M13	C975	10nF	CE(3)		25V	450548
L11	C976	22pF	CE(3)			42412
H11	C977	22pF	CE(3)			42412
H9	C978	56pF	CE(3)			42417
K12	C980	10nF	CE93)		25V	450548
K12	C981	10nF	CE(3)		25V	450548
	DIODES					
M11	D804	4V7	ZENER			33927
H11	D805	4V7	ZENER			33927
L11	D806		Schottky 2811			452034
L11	D807		Schottky 2811			452034
M11	D808		Schottky 2811			452034
L11	D809		Schottky 2811			452034
M11	D810		Schottky 2811			452034
L11	D811		Schottky 2811			452034
K11	D812		IN4148			23802
H11	D813		Schottky 2811			452034
H11	D814		Schottky 2811			452034
H11	D815		Schottky 2811			452034
H11	D816		Schottky 2811			452034
H11	D817		Schottky 2811			452034
H11	D818		Schottky 2811			452034
K11	D819		IN4148			23802
J9	D820		IN823			40045
K11	L801		Ferrite Bead			452760
L9	L802		Ferrite Bead			452760
K10	L803		Ferrite Bead			452760
J9	L804		Ferrite Bead			452760
K12	L805		Ferrite Bead			452760
K9	L806		Ferrite Bead			452760
K9	L807		Ferrite Bead			452760
K10	L808		Ferrite Bead			452760
J11	L809		Ferrite Bead			452760
L11	L810		Ferrite Bead			452760
L9	L811		Ferrite Bead			452760
J9	L812		Ferrite Bead			452760
J8	L813		Ferrite Bead			452760
J9	L814		Ferrite Bead			452760
H8	L815		Ferrite Bead			452760
J9	L816		Ferrite Bead			452760
K8	L817		Ferrite Bead			452760
L9	L818		Ferrite Bead			452760
L10	T801					452271
J10	T802					452271
	TRANSISTORS					
L13	Q801		MPS3640PL			24128
K13	Q802		MPS3640PL			24128
L12	Q803		MPS2369			36625
L12	Q804		MPS2369			36625
M12	Q805		MPS2369			36625
L11	Q806		BFR96			39019
L11	Q807		BSX20			23307
M10	Q808		MPS3640PL			24128
M9	Q809		MPS3640PL			24128
L9	Q810		ZTX327			39271
L10	Q811		BFR96			39019
L10	Q812		BFR96			39019
J13	Q813		MPS3640PL			24128
J13	Q814		MPS2640PL			24128
H12	Q815		MPS2369			36625
H12	Q816		MPS2369			36625
H12	Q817		MPS2369			36625
J11	Q818		BFR96			39019
J11	Q819		BSX20			23307
H9	Q820		MPS3640PL			24128
H9	Q821		MPS3640PL			24128
H9	Q822		ZTX327			39271
J9	Q823		MPS3640PL			24128
J10	Q824		BFR96			39019
J10	Q825		BFR96			39019
	INTEGRATED CIRCUITS					
K13	U840		TL082CP			451262
K8	U841		LF351N			40130
H8	U842		CX20052			451946
L8	U843		CX20052			451946
M10	U844		NPD5566			450919
H10	U845		NPD5566			450919
K8	U846		10216			39903
K10	U847		10101			451809

FAST RAM 4035

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
N1801		Resistor Network 470 x 8			450151
N1802		1k x 8			44892
N1803		1k x 8			44892
N1804		470 x 8			450151
CAPACITORS					
C1801	10nF	CE(2)		25V	450548
C1802	10nF	CE(2)		25V	450548
C1803	10nF	CE(2)		25V	450548
C1804	10nF	CE(2)		25V	450548
C1805	10nF	CE(2)		25V	450548
C1806	10nF	CE(2)		25V	450548
C1807	10nF	CE(2)		25V	450548
C1808	10nF	CE(2)		25V	450548
C1809	10nF	CE(2)		25V	450548
C1810	10nF	CE(2)		25V	450548
C1811	10nF	CE(2)		25V	450548
C1812	10nF	CE(2)		25V	450548
C1813	10nF	CE(2)		25V	450548
C1814	10nF	CE(2)		25V	450548
C1815	10nF	CE(2)		25V	450548
C1816	10nF	CE(2)		25V	450548
C1817	10nF	CE(2)		25V	450548
C1818	10nF	CE(2)		25V	450548
C1819	10nF	CE(2)		25V	450548
C1820	10nF	CE(2)		25V	450548
C1821	10nF	CE(2)		25V	450548
C1822	10nF	CE(2)		25V	450548
C1823	10nF	CE(2)		25V	450548
C1824	10nF	CE(2)		25V	450548
C1825	10nF	CE(2)		25V	450548
C1826	10µF				35931
INTEGRATED CIRCUITS					
U1801		10125			39245
U1802		74LS257			451947
U1803		10125			39245
U1804		10125			39245
U1805		10125			39245
U1806		74LS257			451947
U1807		10125			39245
U1808		10125			39245
U1809		74F374			451966
U1810		MBM2149-45C			451969
U1811		MBM2149-45C			451969
U1812		MBM2149-45C			451969
U1813		MBM2149-45C			451969
U1814		74F374			451966
U1815		10125			39245
U1816		74F157			451950
L1801		Ferrite Bead			452760

Rating	Part No
25V	450548
25V	450548
25V	450548
25V	450548
25V	450548
	35931
	39245
	451947
	39245
	39245
	39245
	451947
	39245
	39245
	451966
	451969
	451969
	451969
	451969
	451966
	39245
	451950
	452760




C1802
C1804 C1805 C1806 C1807 C1808 C1809 C1811 C1813 C1817 C1818 C1820 C1822 C1824 C1825
C1801 C1803 C1810 C1815 C1816
U1802
U1801
U1809
U1808
U1810
U1805
U1811
U1815
U1804
U1812
U1803
N1801
N1801
N1803
N1802
N1802
+5V
-5V
0V
SEL.
OE
WE
CE
Vbb
CLK
TRANS. CLK
WCLK

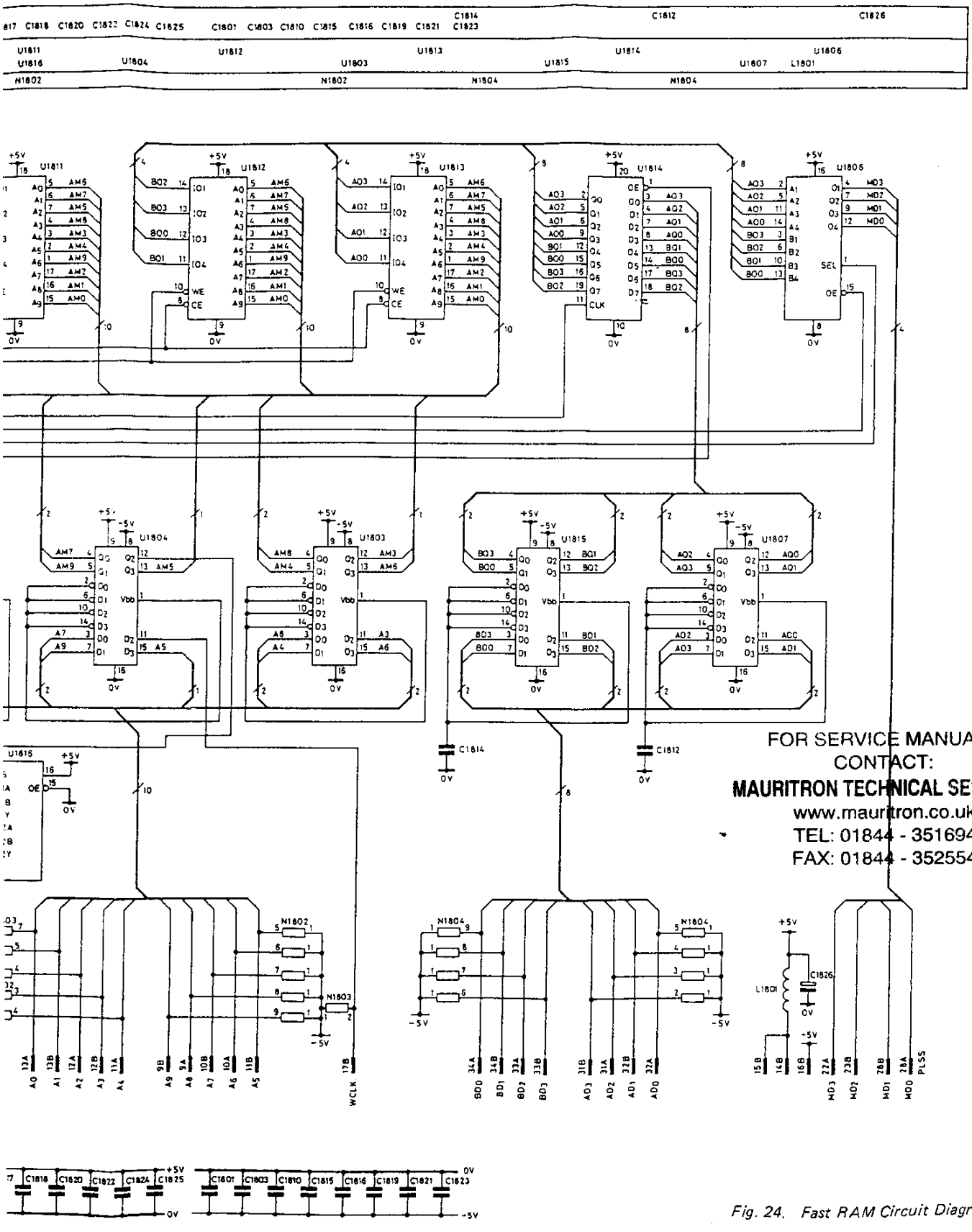


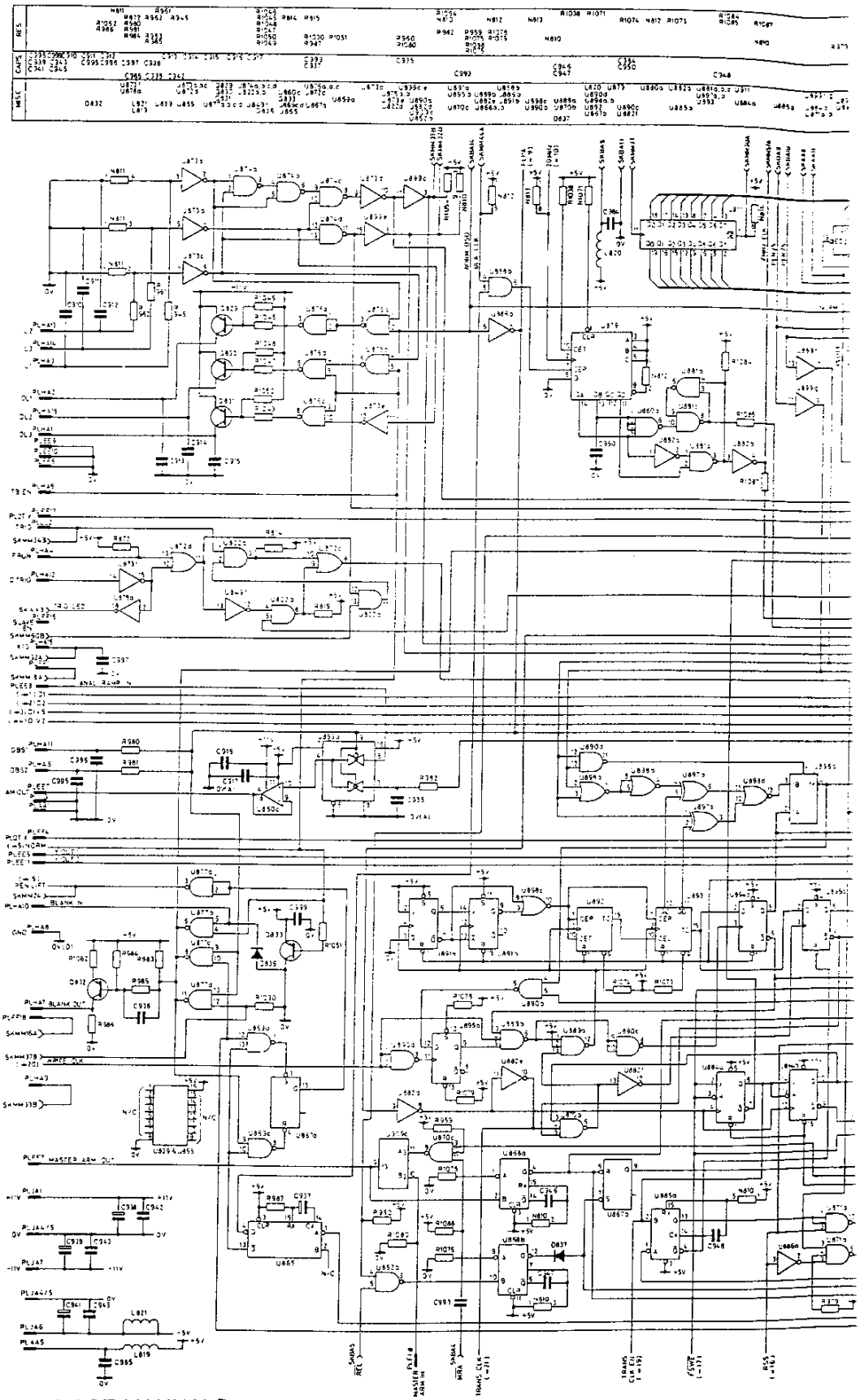
Fig. 24. Fast RAM Circuit Diagram

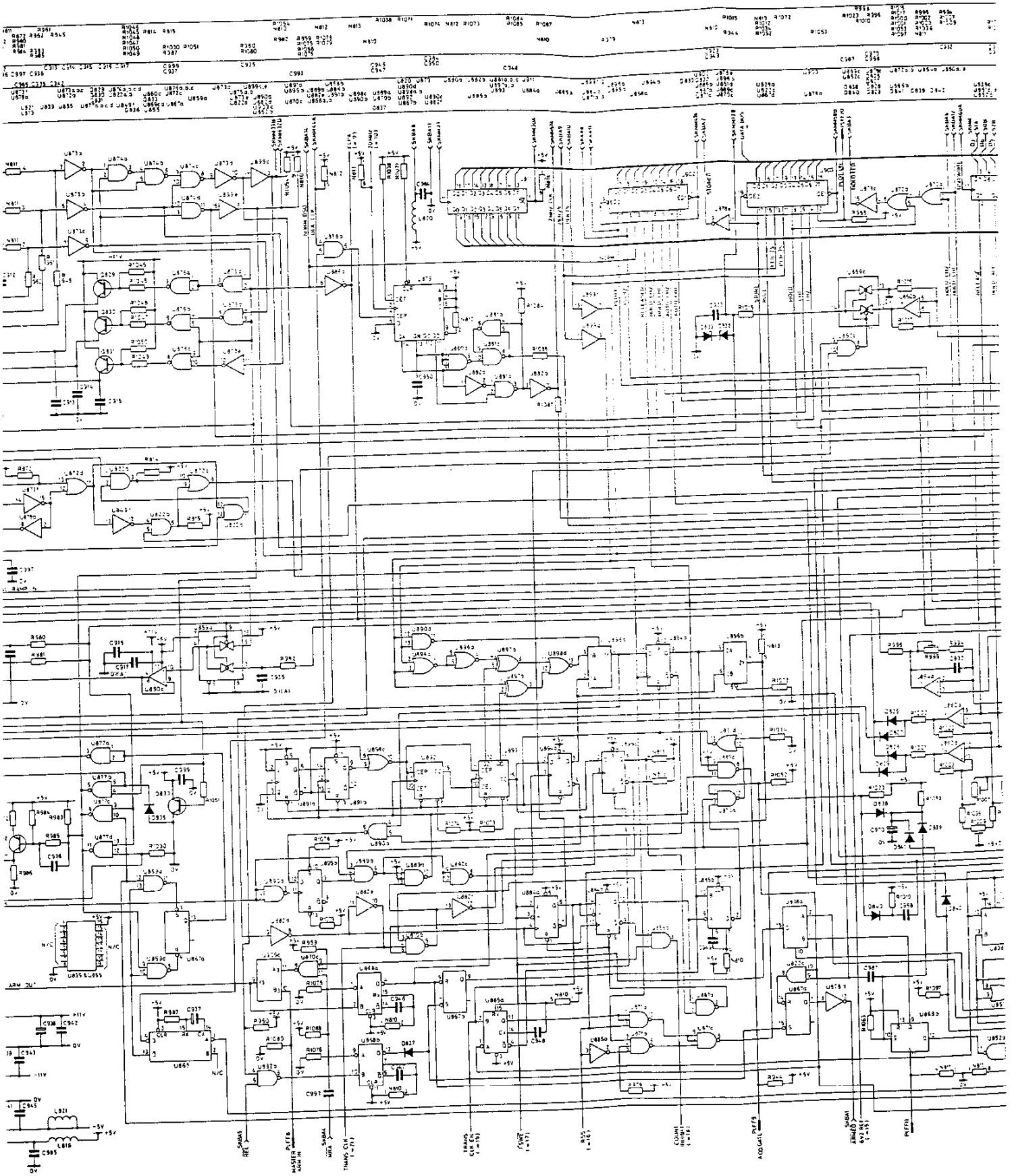
D.S.O. 4035

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
A5	R801	4k7	CF		21805
B5	R802	18k	CF		21811
B12	R803	270	CF		28720
M4	R804	680	CF		28723
M4	R805	1k5	CF		21801
L5	R806	47	CF		28714
K5	R807	1k5	CF		21801
K4	R808	47	CF		28714
M2	R809	1k2	CF		21800
M2	R810	1k5	CF		21801
M2	R811	1k5	CF		21801
H7	R812	1k	CF		21799
J1	R813	820	CF		28724
A2	R814	4k7	CF		21805
A3	R815	4k7	CF		21805
E4	R872	4k7	CF		21805
N802					
L3	N802	1k x 8	Resistor Network		44892
L5	N803	1k x 8	Resistor Network		44892
J4	N810	10k	Resistor Network		450452
E6	N811	10k	Resistor Network		450452
C1	N812	10k	Resistor Network		450452
H1	N813	4k7	Resistor Network		39225
A11	N814	4k7	Resistor Network		39225
K3	N815	1k x 8	Resistor Network		44892
A2	N816	4k7	Resistor Network		39225
J1	R944	47k	CF		21815
E6	R945	10k	CF		21809
H3	R959	4k7	CF		21805
E4	R960	4k7	CF		21805
E6	R961	10k	CF		21809
E6	R962	10k	CF		21809
G5	R979	47k	CF		21815
D1	R980	4k7	CF		21805
E1	R981	4k7	CF		21805
G11	R982	180	CF		21795
J6	R983	1k	CF		21799
J6	R984	1k	CF		21799
J6	R985	3k3	CF		21803
H6	R986	1k	CF		21799
G5	R987	100k	CF		21819
D2	R988	10k	CF		21809
G4	R989	10k	CF		21809
G10	R990	18k	CF		21811
E10	R991	18k	CF		21811
F10	R992	10k	PCP		36267
E10	R993	1k5	CF		21801
F10	R994	1k5	CF		21801
F10	R995	470	PCP		36263
F11	R996	820	CF		28724
G5	R997	100k	CF		21819
F5	R998	100k	CF		21819
E11	R999	22k	CF		21812
F12	R1000	3k	MF	2	38605
G12	R1001	3k	MF	2	38605
F12	R1002	3k9	MF	2	38608
G12	R1003	3k9	MF	2	38608
G10	R1004	220	MF	2	38578
G9	R1005	220	MF	2	38578
F11	R1006	6k8	CF		21807
F11	R1007	10k	PCP		36267
G12	R1008	5k6	CF		21806
G12	R1009	470	PCP		36263
C1	R1010	100k	CF		21819
D4	R1011	10k	CF		21809
E12	R1015	100	CF		21794
F12	R1016	16k	MF	2	38623
F12	R1017	16k	MF	2	38623
C10	R1018	7k5	MF	2	38615
F13	R1019	7k5	MF	2	38615
E9	R1020	6k2	MF	2	38613
E9	R1021	6k2	MF	2	38613
E10	R1022	560	CF		21798
D5	R1023	100k	CF		21819
E13	R1024	100	CF		21794
F11	R1025	6k2	MF	2	38613
E12	R1026	6k2	MF	2	38613
E12	R1027	6k2	MF	2	38613
E12	R1028	6k2	MF	2	38613
F12	R1029	620	MF	2	38589
E8	R1030	470	CF		21797
B7	R1031	47k	CF		21815
D2	R1032	470	CF		21797
G4	R1034	10k	CF		21809
D11	R1035	470	CF		21797
G11	R1036	5k6	CF		21806
H4	R1037	10k	CF		21809
J3	R1038	4k7	CF		21805
F1	R1039	1k5	CF		21801
A2	R1041	470	CF		21797
J2	R1042	220	CF		21796
L1	R1044	470	CF		21797
D6	R1045	22k	CF		21812
D6	R1046	22k	CF		21812
D6	R1047	22k	CF		21812
D6	R1048	22k	CF		21812
E7	R1049	5k6	CF		21806
E8	R1050	22k	CF		21812
D8	R1051	1k	CF		21799
K5	R1052	10k	CF		21809
K4	R1053	100k	CF		21819
C2	R1054	10k	CF		21809

ion 6

ng	Part No
5V	32181
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
5V	32181
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
V	450548
	43498
V	450548
V	32180
V	450548
V	450548
	42436
	43498
	43498
V	450548
	43498
V	450548
	42420
	43498
V	32180
	42432
	42405
V	32180
V	32180
V	32180
/	32180
/	32180
/	450548
/	450548
/	450548
/	450548





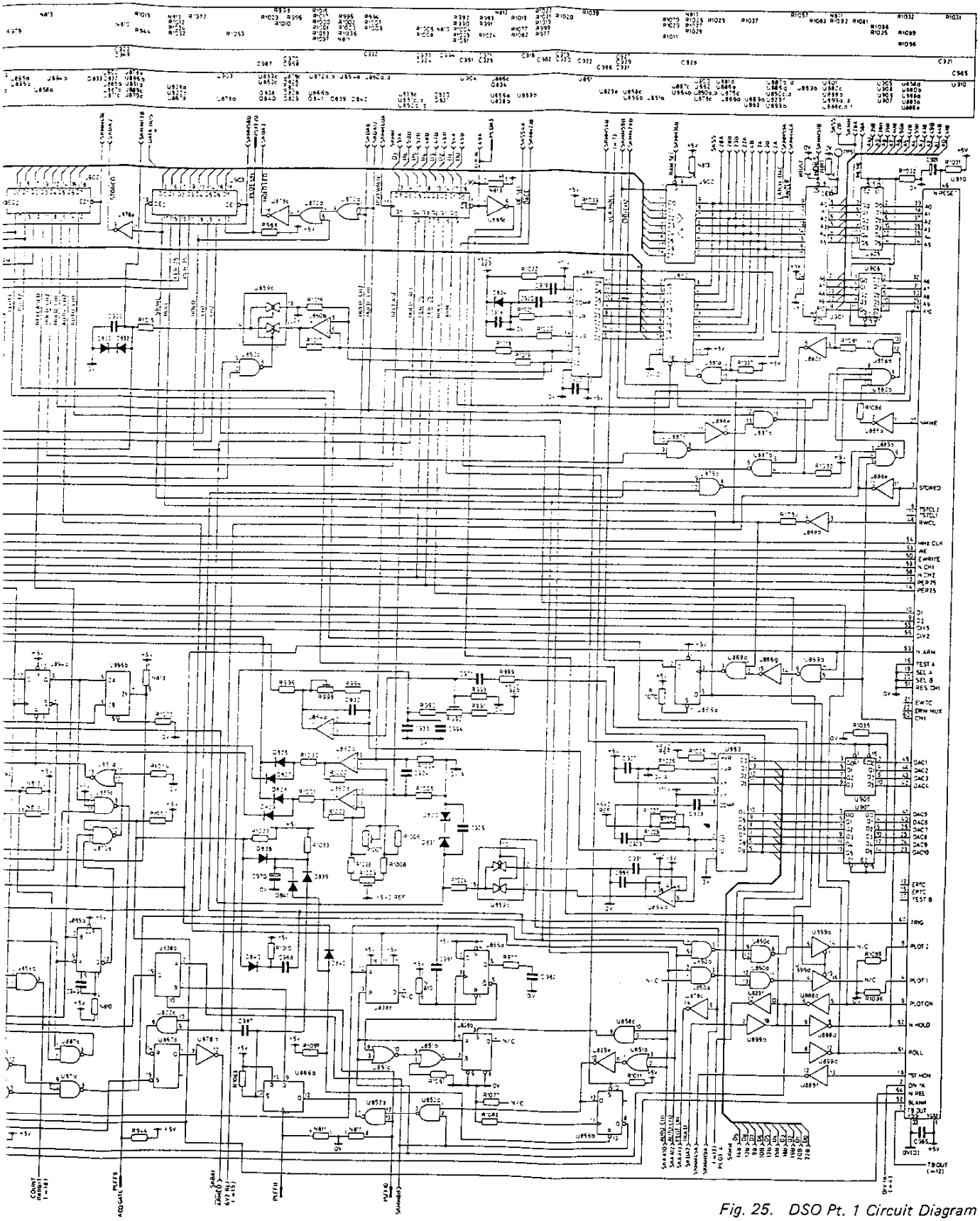


Fig. 25. DSO Pt. 1 Circuit Diagram

D.S.O. 4035 (Cont.)

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS (Cont.)					
R1055	100k	CF			21819
C6 R1057	4k7	CF			21805
B8 R1058	10k	CF			21809
G2 R1059	10k	CF			21809
L1 R1060	220	CF			21796
H4 R1061	10k	CF			21809
H6 R1062	33	CF			28712
E2 R1063	10k	CF			21809
M1 R1064	4k7	CF			21805
D5 R1065	10k	CF			21809
K1 R1066	4k7	CF			21805
L2 R1067	4k7	CF			21805
L2 R1068	330	CF			28721
M2 R1069	330	CF			28721
D3 R1070	10k	CF			21809
J2 R1071	10k	CF			21809
G1 R1072	330	CF			28721
H2 R1073	4k7	CF			21805
H1 R1074	4k7	CF			21805
J5 R1075	10k	CF			21809
J5 R1076	10k	CF			21809
F5 R1077	10k	CF			21809
J2 R1078	4k7	CF			21809
J1 R1079	4k7	CF			21805
K3 R1080	4k7	CF			21805
F2 R1081	150	CF			28719
C1 R1083	330	CF			28721
H3 R1084	2k7	CF			28726
H3 R1085	68	CF			28716
D1 D1086	270	CF			28720
G2 R1087	100	CF			21794
D10 R1088	10k	CF			21809
B1 R1089		Wire Link			
B3 R1090		Not Fitted			
B4 R1091		Not Fitted			
E2 R1092		Not Fitted			
B1 R1093		Not Fitted			
B3 R1096		Wire Link			
G6 R1097	100k	CF			21819
B3 R1098		Not Fitted			
C9 R1099		Not Fitted			
CAPACITORS					
L5 C808	82pF	CE(3)			42419
K4 C809	10pF	CE(3)			42408
M3 C810	10pF	CE(3)			42408
L1 C811	10nF	CE(3)		25V	450548
M4 C812	10nF	CE(3)		25V	450548
L2 C813	10nF	CE(3)		25V	450548
M6 C814	10nF	CE(3)		25V	450548
M7 C815	10nF	CE(3)		25V	450548
M4 C816	10nF	CE(3)		25V	450548

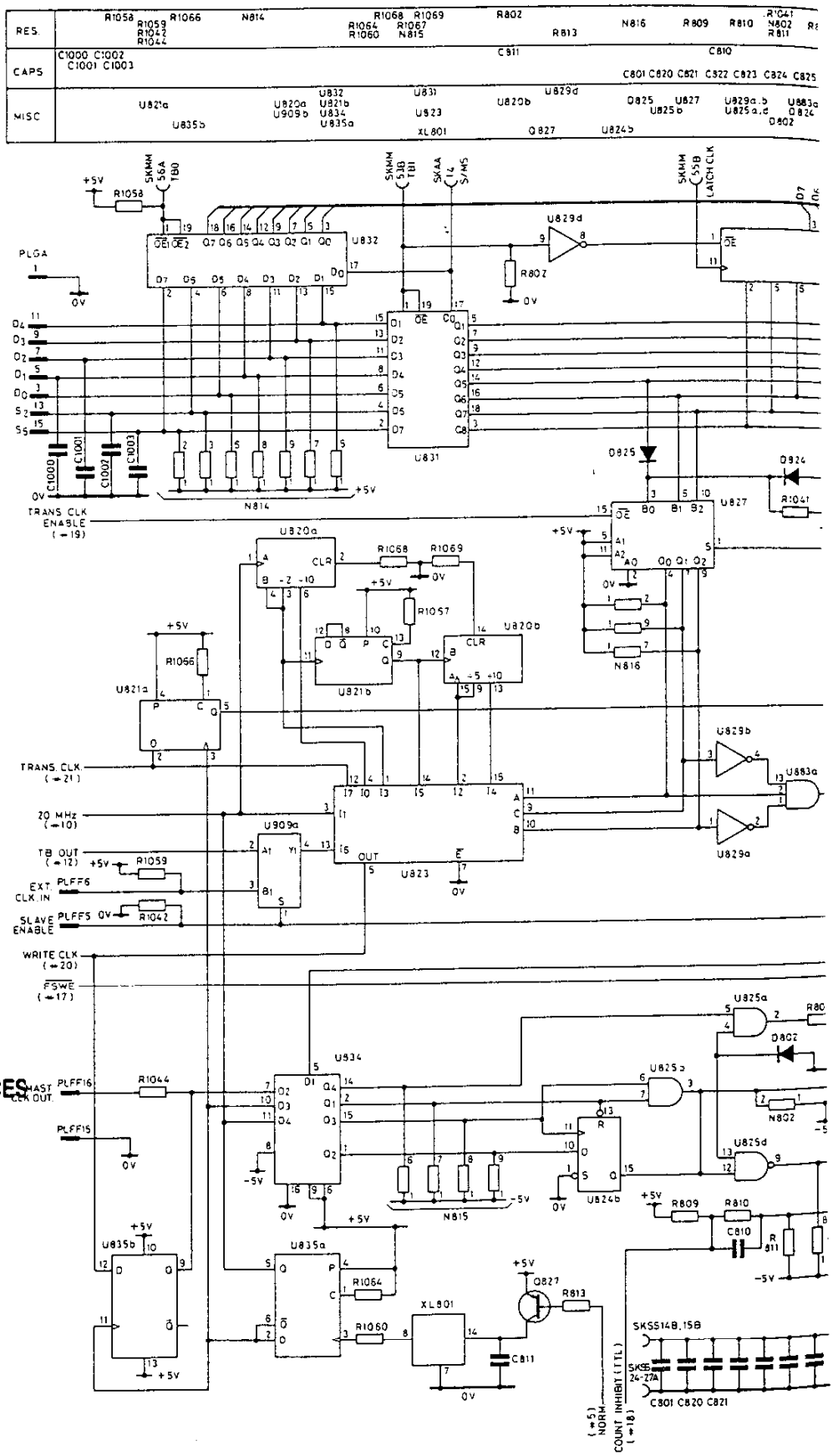
Ref	Value	Description	Tol %±	Rating	Part No
J7 C819	22µF	E		25V	32181
A1 C820	10nF	CE(3)		25V	450548
C1 C821	10nF	CE(3)		25V	450548
E1 C822	10nF	CE(3)		25V	450548
F1 C823	10nF	CE(3)		25V	450548
G1 C824	10nF	CE(3)		25V	450548
H1 C825	10nF	CE(3)		25V	450548
J1 C826	10nF	CE(3)		25V	450548
J1 C827	10nF	CE(3)		25V	450548
L1 C828	10nF	CE(3)		25V	450548
L2 C829	10nF	CE(3)		25V	450548
K2 C830	10nF	CE(3)		25V	450548
J2 C831	10nF	CE(3)		25V	450548
B6 C832	10nF	CE(3)		25V	450548
G6 C833	10nF	CE(3)		25V	450548
L7 C834	22µF	E		25V	32181
K10 C906	10nF	CE(3)		25V	450548
K9 C907	10nF	CE(3)		25V	450548
D7 C910	10nF	CE(3)		25V	450548
D8 C911	10nF	CE(3)		25V	450548
D7 C912	10nF	CE(3)		25V	450548
D7 C913	10nF	CE(3)		25V	450548
D7 C914	10nF	CE(3)		25V	450548
D8 C915	10nF	CE(3)		25V	450548
F12 C916	10nF	CE(3)		25V	450548
G12 C917	10nF	CE(3)		25V	450548
E10 C918	10nF	CE(3)		25V	450548
E9 C919	100nF	CE(3)			43498
E10 C920	10nF	CE(3)		25V	450548
B8 C921	10µF	CE(3)		25V	32180
G9 C922	10nF	CE(3)		25V	450548
D12 C923	10nF	CE(3)		25V	450548
G10 C924	2.2nF	CE(3)			42436
E13 C925	100nF	CE(3)			43498
E12 C927	100nF	CE(3)			43498
E12 C928	10nF	CE(3)		25V	450548
F12 C929	100nF	CE(3)			43498
G10 C931	10nF	CE(3)		25V	450548
F11 C932	100pF	CE(3)			42420
G10 C933	100nF	CE(3)			43498
F6 C934	10µF	E		25V	32180
F12 C935	1nF	CE(3)			42432
H5 C936	5.6pF	CE(3)			42405
H5 C937	10µF	E		25V	32180
F13 C938	10µF	E		25V	32180
D13 C939	10µF	E		25V	32180
D13 C940	10µF	E		25V	32180
F13 C941	10µF	E		25V	32180
E13 C942	10nF	CE(3)		25V	450548
D12 C943	10nF	CE(3)		25V	450548
E13 C944	10nF	CE(3)		25V	450548
E13 C945	10nF	CE(3)		25V	450548

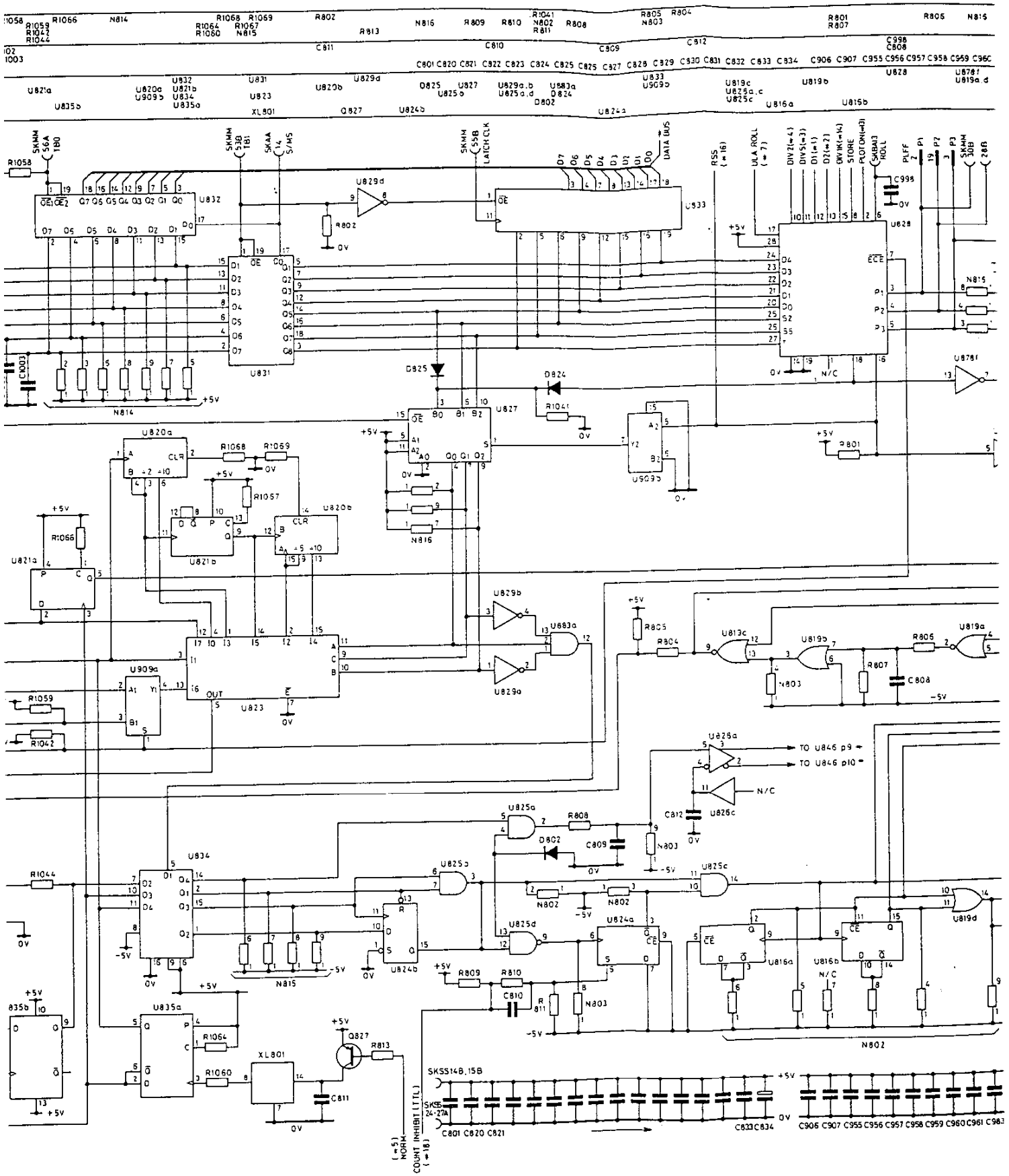
D.S.O. 4035 (Cont.)

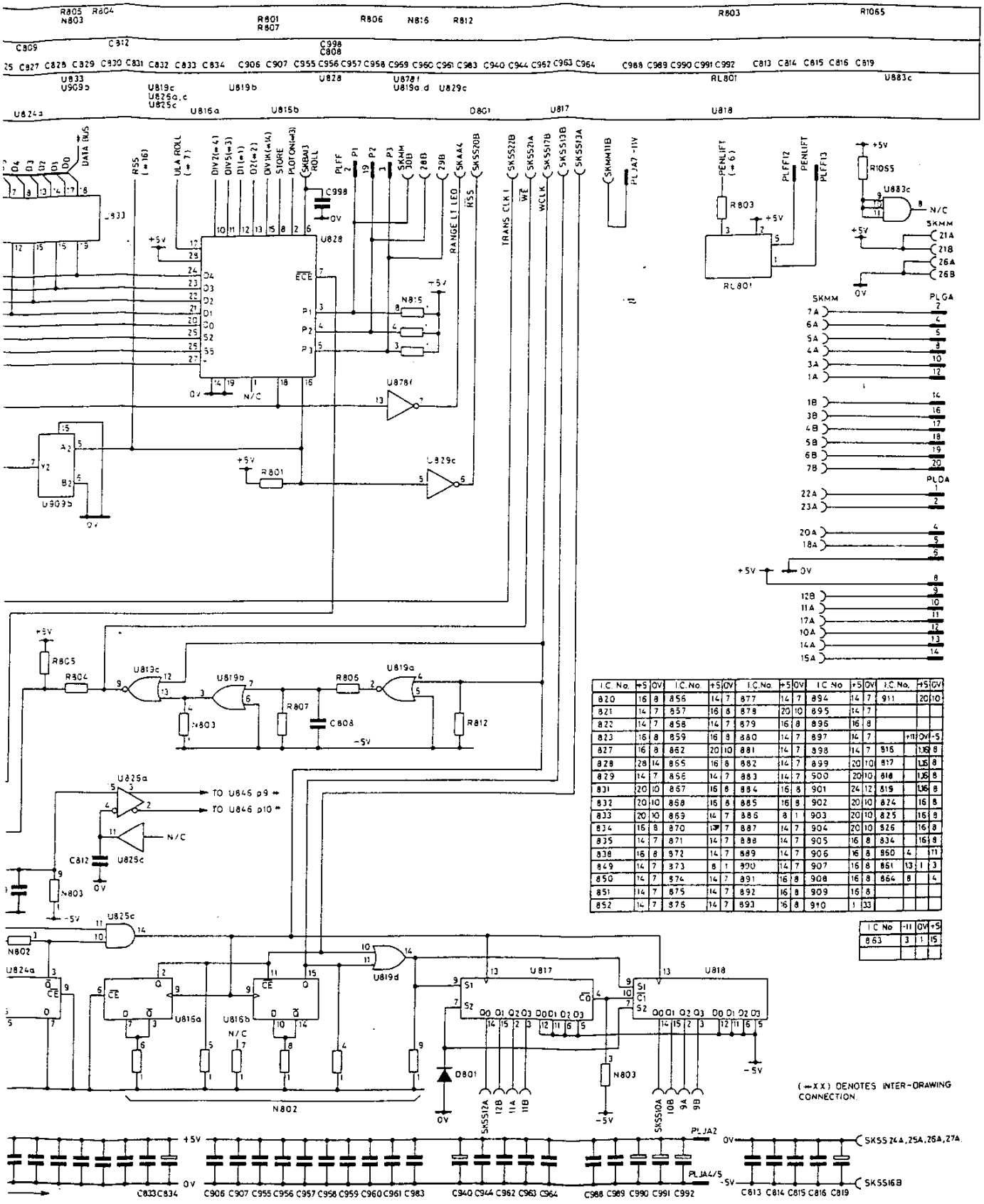
Ref	Value	Description	Tol %±	Rating	Part No
CAPACITORS (Cont.)					
J4	C946	10nF	CE(3)	25V	450548
J5	C947	10nF	CE(3)	25V	450548
J3	C948	10nF	CE(3)	25V	450548
J4	C949	10nF	CE(3)	25V	450548
J2	C950	18pF	CE(3)		42411
J3	C951	1nF	CE(3)		42432
F5	C953	10µF	E	25V	32180
B6	C955	10nF	CE(3)	25V	450548
A10	C956	10nF	CE(3)	25V	450548
B8	C957	10nF	CE(3)	25V	450548
D1	C958	10nF	CE(3)	25V	450548
K6	C959	10nF	CE(3)	25V	450548
H6	C960	10nF	CE(3)	25V	450548
D10	C961	10nF	CE(3)	25V	450548
D5	C962	10nF	CE(3)	25V	450548
F2	C963	10nF	CE(3)	25V	450548
G2	C964	10nF	CE(3)	25V	450548
C1	C965	10nF	CE(3)	25V	450548
G4	C966	220pF	CE(3)		42424
D2	C968	1nF	CE(3)		42432
K4	C970	10µF	E	25V	32180
E11	C971	5.6pF	CE(3)		42405
H3	C983	10nF	CE(3)	25V	450548
C10	C984	10nF	CE(3)	25V	450548
C9	C985	10nF	CE(3)	25V	450548
F11	C986	10nF	CE(3)	25V	450548
E3	C987	10nF	CE(3)	25V	450548
J3	C988	10nF	CE(3)	25V	450548
D1	C989	10nF	CE(3)	25V	450548
A5	C990	10µF	CE(3)	25V	32180
C8	C991	10µF	CE(3)	25V	32180
E5	C992	10µF	CE(3)	25V	32180
D10	C993	4.7nF	CE(3)		42440
E7	C995	10nF	CE(3)	25V	450548
E7	C996	10nF	CE(3)	25V	450548
E8	C997	10nF	CE(3)	25V	450548
D10	C998	10nF	CE(3)	25V	450548
A11	C1000	10nF	CE(3)	25V	450548
A11	C1001	10nF	CE(3)	25V	450548
A11	C1002	10nF	CE(3)	25V	450548
A11	C1003	10nF	CE(3)	25V	450548
DIODES					
K6	D801		IN4148		23802
L5	D802		IN4148		23802
A3	D824		OA47		4468
A1	D825		OA47		4468
G11	D826		IN4148		23802
G15	D827		IN4148		23802
G11	D828		IN4148		23802
G13	D829		IN4148		23802
E13	D830	3V9	ZENER		33925
E13	D831	3V9	ZENER		33925
D12	D832	3V9	ZENER		33925
D12	D833	3V9	ZENER		33925
F10	D834		IN823		40045
D8	D836		IN4148		23802
K5	D837		IN4148		23802
K4	D838		IN4148		23802
E3	D839		OA47		4468
C2	D840		IN4148		23802
H5	D841		IN4148		23802
H5	D842		IN4148		23802
TRANSISTORS					
L1	Q827		BSX29		25740
D7	Q829		2N3906		21533
D6	Q830		2N3906		21533
D7	Q831		2N3906		21533
H5	Q832		2N3906		21533
D8	Q833		2N3906		21533
C8	L819		Ferrite Bead		452760
C10	L820		Ferrite Bead		452760
G8	L821		Ferrite Bead		452760
C12	RL801		GT831A		43961
K1	XL801		40MHz XTAL. OSC.		452554
INTEGRATED CIRCUITS					
J6	U816		10131		39246
L6	U817		10136		450952
L6	U818		10136		450952
L5	U819		10103		40346
M1	U820		74LS390		43675
L1	U821		74ALS74		451308
A3	U822		74LS08		36467
K1	U823		74LS151		41085
L2	U824		10131		39246
L3	U825		10104		41064
M4	U826		10216		39903
A1	U827		74LS257		451947
A2	U828		82S100FPLA		451944
B5	U829		74HC04		451958
A11	U831		MM74C244NS		450913
C9	U832		MM74C244NS		450913
A8	U833		MM74C374NS		451266
L3	U834		10124		44366
L1	U835		74F74		451948
H6	U838		4053		41891
E1	U839		Not Fitted		

ction 6

Rating	Part No
	451956
	451958
	452422
	451963
	451267
	36200
	451956
	451958
	451303
	451299
	451951
	451312
	451312
	451308
	451308
	36735
	38421
	44384
	450913
	451953
	450683
	450913
	450913
	451266
	41295
	41295
	41295
	41295
	451964
	450600
	451266




R1058
R1059
R1066
N814
R1042
R1044
R1068
R1069
R1064
R1067
R1060
N815
R802
R813
N816
R809
R810
R1041
N802
R811
R808
R805
R804
N803
R801
R807
R806
N815
C811
C810
C809
C812
C998
C808
C801 C820 C821 C822 C823 C824 C825 C826 C827 C828 C829 C830 C831 C832 C833 C834 C906 C907 C955 C956 C957 C958 C959 C960
U821a
U835b
U820a
U909b
U832
U821b
U834
U835a
U831
U823
XL801
U820b
U829d
Q827
U824b
D825
U827
D824
U824a
U825b
U827
U829a,b
U825a,d
U683a
D802
U833
U909b
U819c
U825a,c
U825c
U816a
U819b
U815b
U828
U878f
U819a,d
SKMM 56A 180
SKMM 53B 181
SKAA 14 S/MS
SKMM 55B LATCH CLK
DATA BUS
RSS (÷16)
ULA ROLL (÷7)
DIV2(÷4)
DIV5(÷3)
D1(÷1)
D2(÷2)
DIV10(÷10)
STORE
PLOT(N=0)
SKBAN3 ROLL
PLFF
SKMM 30B
28B
CK003
+5V
0V
N/C
U820a
U820b
U821b
U821a
U829b
U829a
U823
U909a
U813c
U819b
U819a
U826a
TO U846 p9
TO U846 p10
U826c
U825a
U825b
U825c
U825d
U824a
U824b
U834
U835a
U816a
U816b
U819d
N802
N803
N815
R1064
R1060
R1057
R1066
R1059
R1042
R1044
R809
R810
R811
C810
C809
C808
C812
C811
Q827
R813
XL801
SKSS14B,15B
SKSS 24+27A
C801 C820 C821
C833 C834
C906 C907 C955 C956 C957 C958 C959 C960 C961 C983
(+5) NORM
COUNT INHIBIT (TTL) (÷18)



I.C. No.	+5	0V	I.C. No.	+5	0V	I.C. No.	+5	0V	I.C. No.	+5	0V	I.C. No.	+5	0V
820	16	8	856	14	7	877	14	7	894	14	7	911	20	10
821	14	7	857	16	8	878	20	10	895	14	7			
822	14	7	858	14	7	879	16	8	896	16	8			
823	16	8	859	16	8	880	14	7	897	14	7		+11	0V -5
827	16	8	862	20	10	881	14	7	898	14	7	915		LS 8
828	28	14	865	16	8	882	14	7	899	20	10	917		LS 8
829	14	7	866	14	7	883	14	7	900	20	10	918		LS 8
831	20	10	867	16	8	884	16	8	901	24	12	919		LS 8
832	20	10	868	16	8	885	16	8	902	20	10	824		16 8
833	20	10	869	14	7	886	8	1	903	20	10	825		16 8
834	16	8	870	14	7	887	14	7	904	20	10	826		16 8
835	14	7	871	14	7	888	14	7	905	16	8	834		16 8
838	16	8	872	14	7	889	14	7	906	16	8	850	4	11
849	14	7	873	8	1	900	14	7	907	16	8	851	13	1 3
850	14	7	874	14	7	891	16	8	908	16	8	864	8	4
851	14	7	875	14	7	892	16	8	909	16	8			
852	14	7	876	14	7	893	16	8	910	1	33			

I.C No	-11	0V	+5
863	3	1	15

Fig. 26. DSO Pt. 2 Circuit Diagram

D.S.O. 4035 (Cont.)

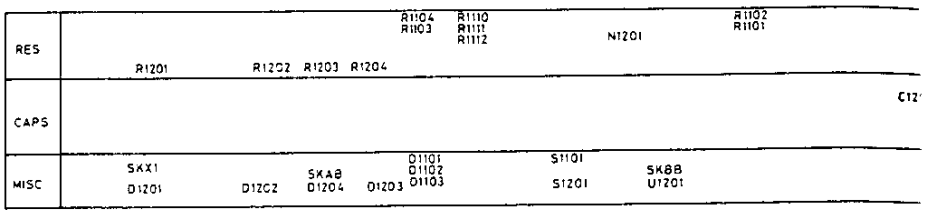
Ref	Value	Description	Tol %±	Rating	Part No
B1	U849	74HC04			451958
D5	U850	74C00			451282
F4	U851	74HC02			451957
F4	U852	74C00			451282
C11	U855	Not Fitted			
E5	U856	74C74			451290
F1	U858	74HC08			451959
E12	U859	4053			41891
F12	U860	LF347N			450908
F9	U861	LMDAC08H			450686
F8	U862	74C374			451266
E11	U863	A–D CONVERTOR			451945
F11	U864	TL082CP			451262
G5	U865	74C221			451267
E3	U866	74C74			451290
H4	U867	4044			44024
K5	U868	74C221			451267
H5	U869	74C00			451282
G3	U870	74HC10			451960
G4	U871	74HC10			451960
B2	U872	74HC32			452265
E6	U873	4049			36200
F6	U874	74C00			451282
G6	U875	74C00			451282
D6	U876	74LS26			44362
E8	U877	74ALS1003			451970
D9	U878	MM74C240NS			451326
J2	U879	74HC160			451965
H3	U880	74HC20			451961
H3	U881	74HC00			451956
H3	U882	74HC04			451958
C5	U883	74HC11			452422
J5	U884	74HC109			451963
J4	U885	74C221			451267
E1	U886	4049			36200
F3	U887	74HC00			451956
D1	U888	74HC04			451958
J1	U889	74ALS10			451303
J1	U890	74AlS00			451299
J1	U891	74ALS109			451951
H1	U892	74ALS161			451312
H2	U893	74ALS161			451312
G2	U894	74ALS74			451308
J2	U895	74ALS74			451308
G1	U896	74LS157			36735
G1	U897	74LS86			38421
G1	U898	74F02			44384
E2	U899	MM74C244NS			450913
A8	U900	74ALS245			451953
C7	U901	HM6116P–3			450683
B1	U902	74C244			450913
D2	U903	74C244			450913
D4	U904	74374			451266
C7	U905	4503			41295
C10	U906	4503			41295
D11	U907	4503			41295
C6	U908	4503			41295
K3	U909	74HC157			451964
C3	U910	ULA			450600
E10	U911	74C374			451266

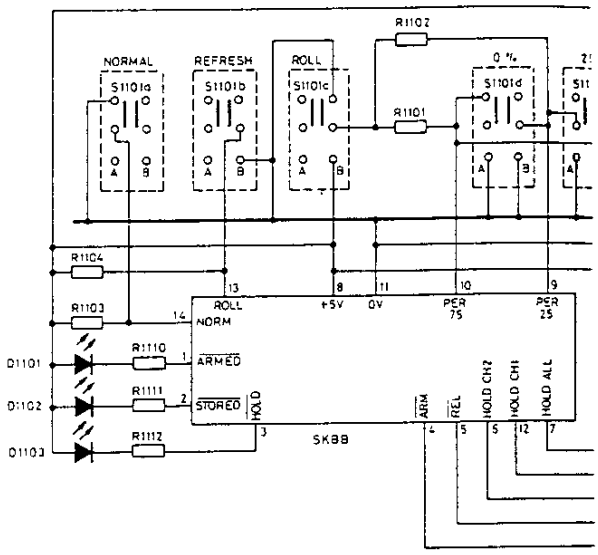
FUNCTION PICK-OFF & PLOT SWITCH 4035

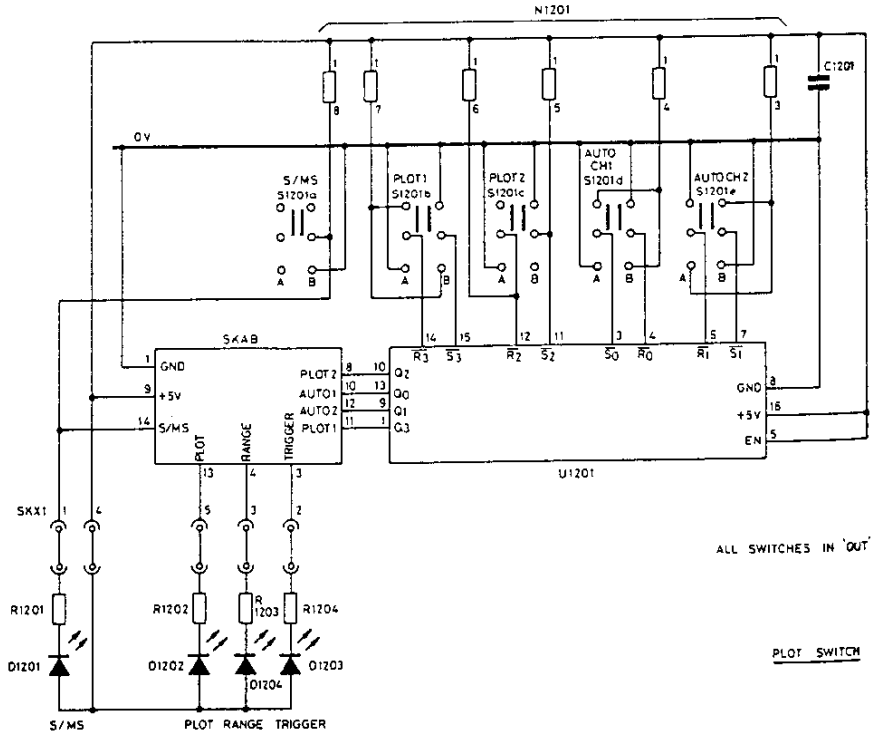
Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R1101	10k	CF			21809
R1102	10k	CF			21809
R1103	10k	CF			21809
R1104	10k	CF			21809
R1105	10k	CF			21809
R1106	10k	CF			21809
R1107	10k	CF			21809
R1108	10k	CF			21809
R1109	10k	CF			21809
R1110	270	CF			28720
R1111	270	CF			28720
R1112	270	CF			28720
R1201	270	CF			28720
R1202	270	CF			28720
R1203	270	CF			28720
R1204	270	CF			28720
N1201	10k	Resistor Network			450452
CAPACITORS					
C1101	10nF	CE(3)		25V	450548
C1201	10nF	CE(3)		25V	450548
C1401	10nF	CE(3)		25V	450548
C1402	10nF	CE(3)		25V	450548
C1403	10nF	CE(3)		25V	450548
C1404	10nF	CE(3)		25V	450548
C1405	10nF	CE(3)		25V	450548
C1406	10nF	CE(3)		25V	450548
C1407	10nF	CE(3)		25V	450548
C1408	10nF	CE(3)		25V	450548
C1409	10nF	CE(3)		25V	450548
C1410	10nF	CE(3)		25V	450548
C1411	10nF	CE(3)		25V	450548
C1412	10nF	CE(3)		25V	450548
C1413	10nF	CE(3)		25V	450548
C1414	10nF	CE(3)		25V	450548
C1415	10nF	CE(3)		25V	450548
C1416	10nF	CE(3)		25V	450548
C1417	10nF	CE(3)		25V	450548
C1418	10nF	CE(3)		25V	450548
C1419	10nF	CE(3)		25V	450548
DIODES					
D1101		LED			43847
D1102		LED			43847
D1103		LED			43847
D1201		LED			43847
D1202		LED			43847
D1203		LED			43847
D1204		LED			43847
INTEGRATED CIRCUITS					
U1101		4044			44024
U1102		4044			44024
U1201		4044			44024
MISCELLANEOUS					
S1101					452242
S1201					452248
S1401					453156
S1402					452891
S1403					452891

tion 6

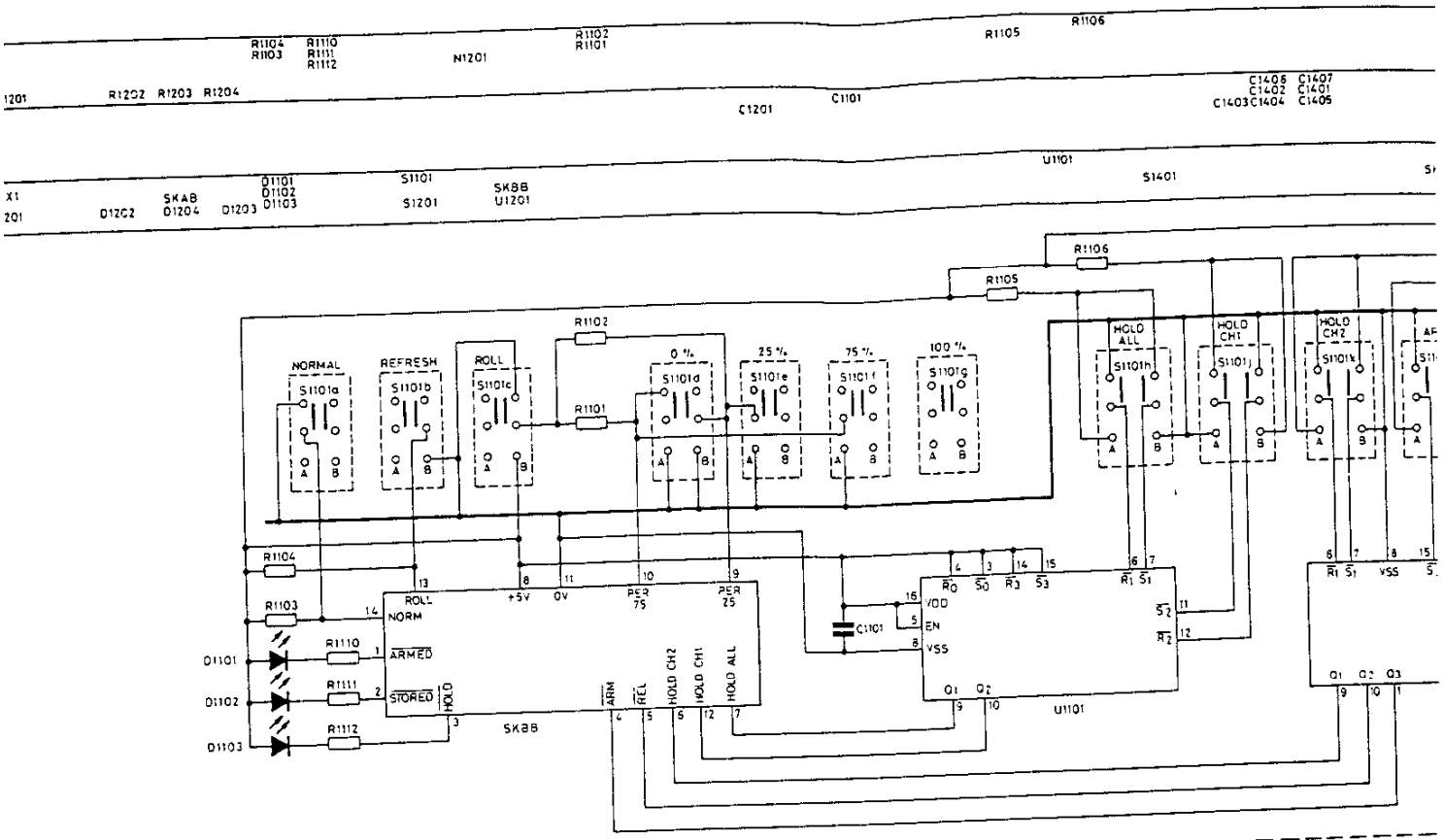
iting	Part No
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
5V	450548
	43847
	43847
	43847
	43847
	43847
	43847
	43847
	44024
	44024
	44024
	452242
	452248
	453156
	452891
	452891

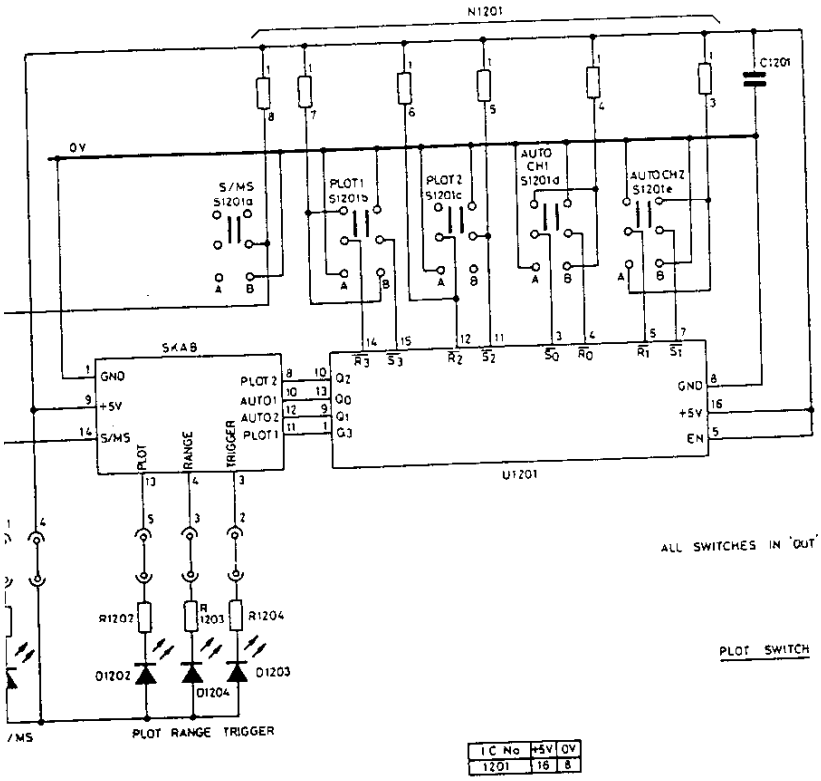






I C No	+5V	0V
1201	16	8

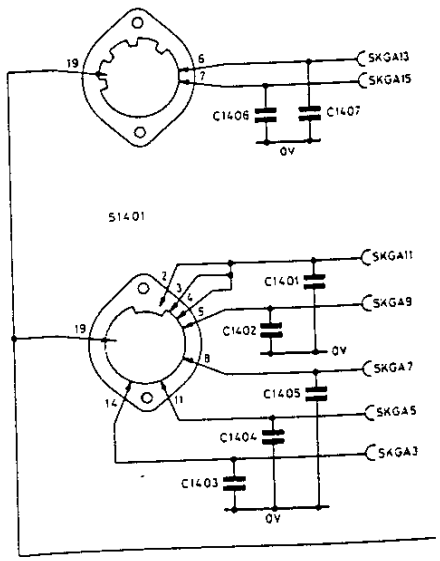




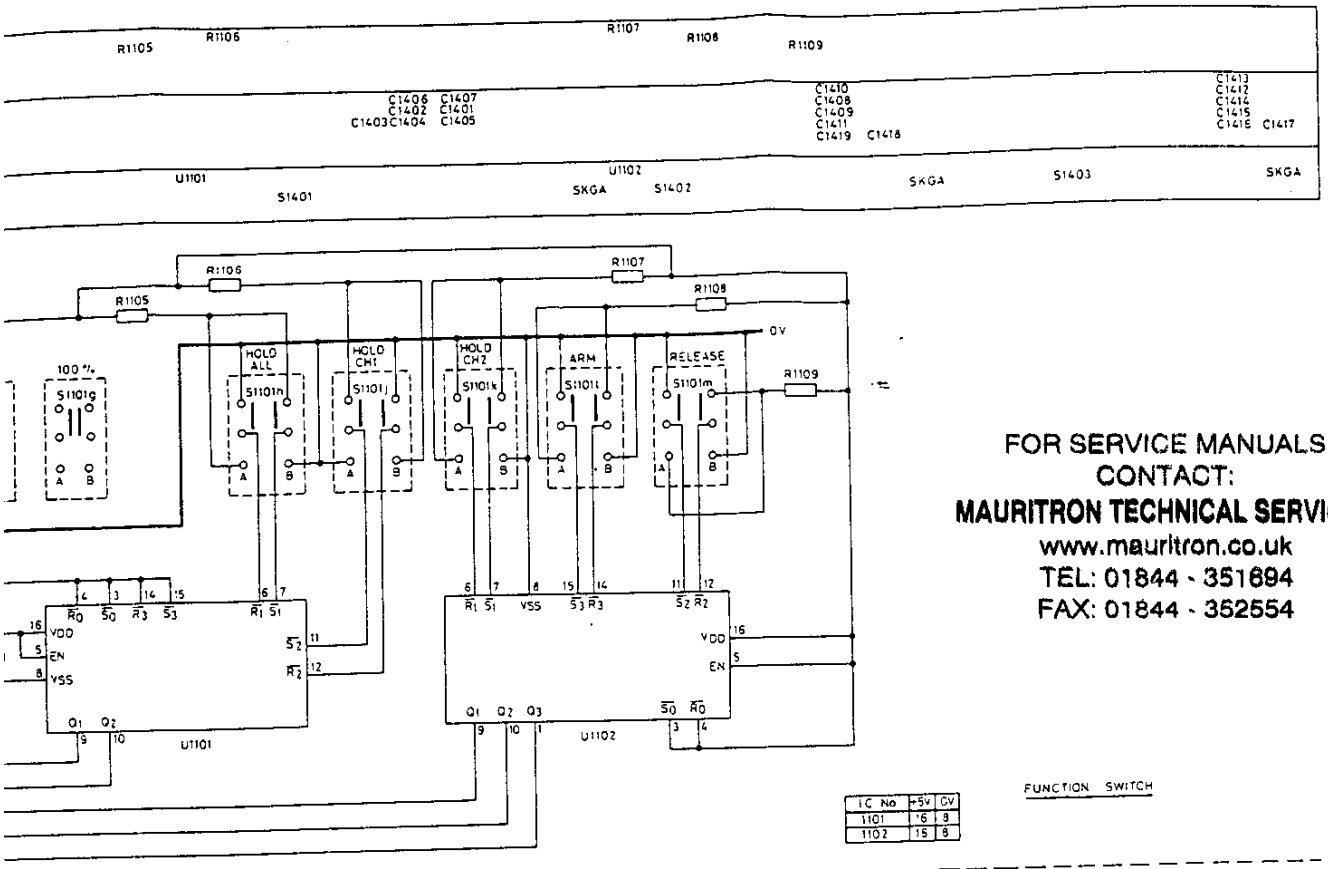
ALL SWITCHES IN 'OUT' POSITION

PLOT SWITCH

I C No	+5V	0V
1201	16	8



PICK - OFF SWITCH



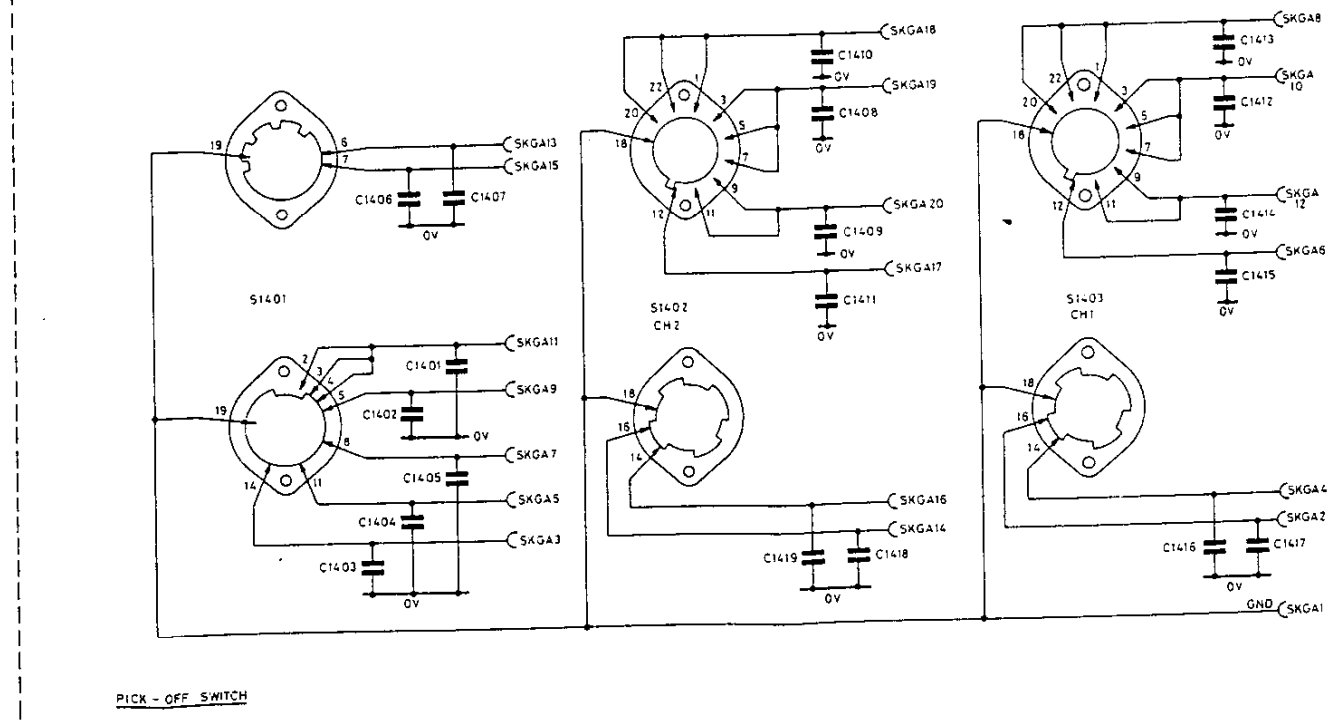


Fig. 27. Function, Pick-off and Plot Switch Circuit Diagram

POWER SUPPLY 4035 (ANALOGUE PCB)

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R558	10	CF			21793
R574	12k	CF		1W	19051
R575	12k	CF		1W	19051
R701	1k	CF			21799
R702	680	CF			28723
R703	10k	CC	5	1W	2882
R704	22k	CF			21812
R705	5k6	CF			21806
R706	470	CF			21797
R707	8k2	CF			21808
R708	220k	PCP			36270
R710	2k2	CF			21802
R713	470k	PCP			36271
R714	1M5	CF		½W	18588
R715	680k	CF			21839
R716	33M	MG	5	½W	43008
R717	33M	MG	5	½W	43008
R718	22k	CC		¼W	3433
R719	18k	CF		½W	18565
R721	180	CF		½W	18541
R722	1k	CF			21799
R723	2k2	CF			21802
R724	5k6	CF			21806
R725	47k	PCP			38261
R726	33k	MF	2		38630
R727	120	CF			28718
R728	33k	CF			28712
R729	680	CF			28723
R730	1k	CF			21799
R731	10k	MF	2		38618
R732	47k	CF			21815
R733	22k	CF	10		3433
R734	1k5	CF			21801
R735	10k	PCP			452628
R736	1k	CF			21799
R737	10k	PCP			44959
R738	180	MF	2		38576
R739	47	CF			18534
R741	5k6	CC	5	1W	2363
R742	220k	MF	2		38650
R743	33M	MG	5	½W	43008
R744	1M	CP			44460
R745	10k	CP			44461
R746	82k	CF			21818
R747	120k	CF			21820
R748	100k	CF			21819
N720		Resistor Network			44608

Ref	Value	Description	Tol %±	Rating	Part No
CAPACITORS					
C512	5.6nF	CE(2)			22394
C701	10nF	CE(2)		25V	450548
C702	2200pF	CE(2)		4kV	44990
C703	2200pF	CE(2)		4kV	44990
C705	33µF	CE(2)		350V	44991
C708	10µF	E		25V	32180
C709	5.6nF	CE(2)		4kV	43117
C710	10µF	E		25V	32180
C711	0.1µF	PE		1500V	40075
C712	0.1µF	PE		1500V	40075
C713	0.22µF	MF		100V	44370
C714	10nF	CE(2)		25V	450548
C715	10nF	CE(2)		25V	450548
C716	10nF	CE(2)		25V	450548
C717	56pF	CE(3)			42417
C718	22pF	CE(3)			42412
C719	5.6nF	CE(2)			22394
C720	5.6pF			50V	42405
C721		Track Capacitance			
DIODES					
D701		IN4148			23802
D702		IN4148			23802
D704		LED			43847
D705		BAY17			402022
D706		ZENER		150V	37559
D708		IN4148			23802
D709		ZENER		200V	40052
D712		ZENER		5V1	33928
D715		ZENER		200V	40052
D716		ZENER		200V	40052
D717		ZENER		200V	40052
D718		1JK60TR			451803
D719		1JK60TR			451803
D720		IN4148			23802
D721		BAX17			402022
D722		IN4004			450266
D723		IN4004			450266
D724		IN4004			452066
D725		IN4004			450266
D730		ZENER		200V	40052
TRANSISTORS					
Q701		TJ630			44953
Q702		BFR86B			44954
Q703		BFR86B			44954
Q704		BC558C			44952

POWER SUPPLY 4035 (ANALOGUE PCB) (Cont.)

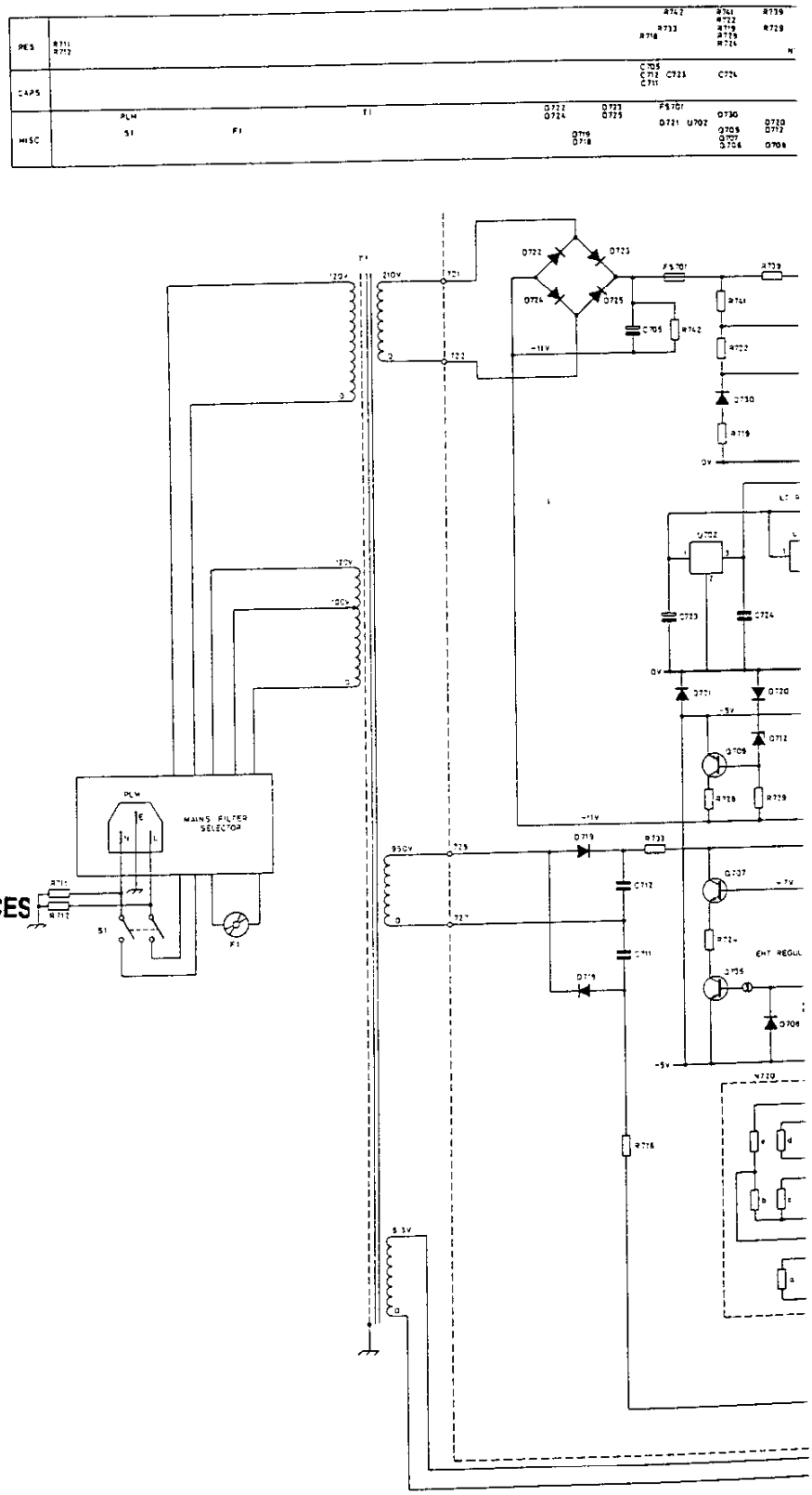
Ref	Value	Description	Tol %±	Rating	Part No
Q706		BC547B			44951
Q707		BUX87			44955
Q709		BC328			38414
Q711		BC558C			44952
Q713		TIP112			40591
Q714		BC547B			44951
Q715		BC557B			44950
Q716		2N6518			36472
Q717		MPS2369			36625
MISCELLANEOUS					
U701					40060
V1		56840GY/93			452926
FS701					4732
LP701					40328
LP702					40328
L1					44993
S701					38729
T1					452589
L403		Choke			44993
L404		Choke			44993

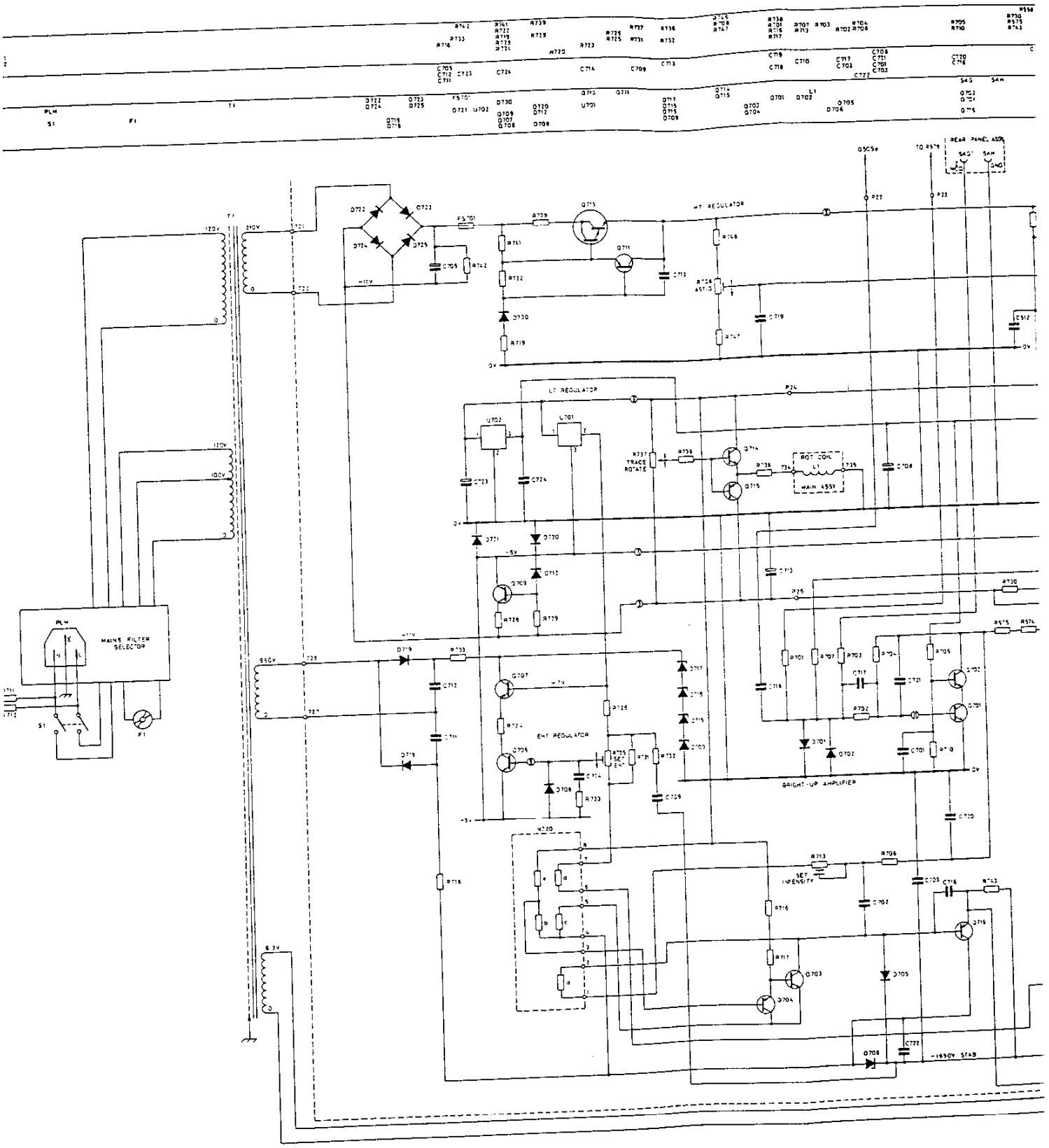
POWER SUPPLY 4035

Ref	Value	Description	Tol %±	Rating	Part No
RESISTORS					
R1302	300	MF	2		38581
R1303	100	MF	2		38570
R1304	150	MF	2		38574
R1305	1k2	MF	2		38596
R1306	1k2	MF	2		38596
R1307	150	MF	2		38574
R1309	100k	CF			21819
CAPACITORS					
C1301	6800µF	E		16V	450796
C1302	6800µF	E		16V	450796
C1303	100nF	CE(3)		50V	43498
C1304	6800µF	E		16V	450796
C1305	100nF	CE(3)		50V	43498
C1306	1µF	T		35V	34895
C1307	1µF	T		35V	34895
C1309	3300µF	E		25V	44578
C1310	100nF	CE(3)		50V	43498
C1311	3300µF	E		25V	44578
C1312	100nF	CE(3)		50V	43498
C1313	1µF	T		35V	34895
C1314	1µF	T		35V	34895
C1317	100nF	CE(3)		50V	43498
DIODES					
D1301		IN5402			51382
D1302		IN5402			51382
D1303		IN4003			23462
D1304		IN4003			23462
D1305		IN4003			23462
D1306		IN4003			23462
D1307		IN5402			51382
D1308		IN5402			51382
INTEGRATED CIRCUITS					
U1301		BY255-100		100V	451943
U1302		LM323K			47059
U1303		LM337T			44842
U1304		LM317			40731
U1305		LM337T			44842

tion 6

ting	Part No
	452926
	4732
	40328
	40328
	44993
	38729
	452589
	44993
	44993




MAINS FILTER SELECTOR
HT REGULATOR
LT REGULATOR
EHT REGULATOR
BRIGHT-UP AMPLIFIER
TRACE ROTATE
ROT COIL
MAIN ASSY
REAR PANEL ASSY
SET INTENSITY
-1650V STAB

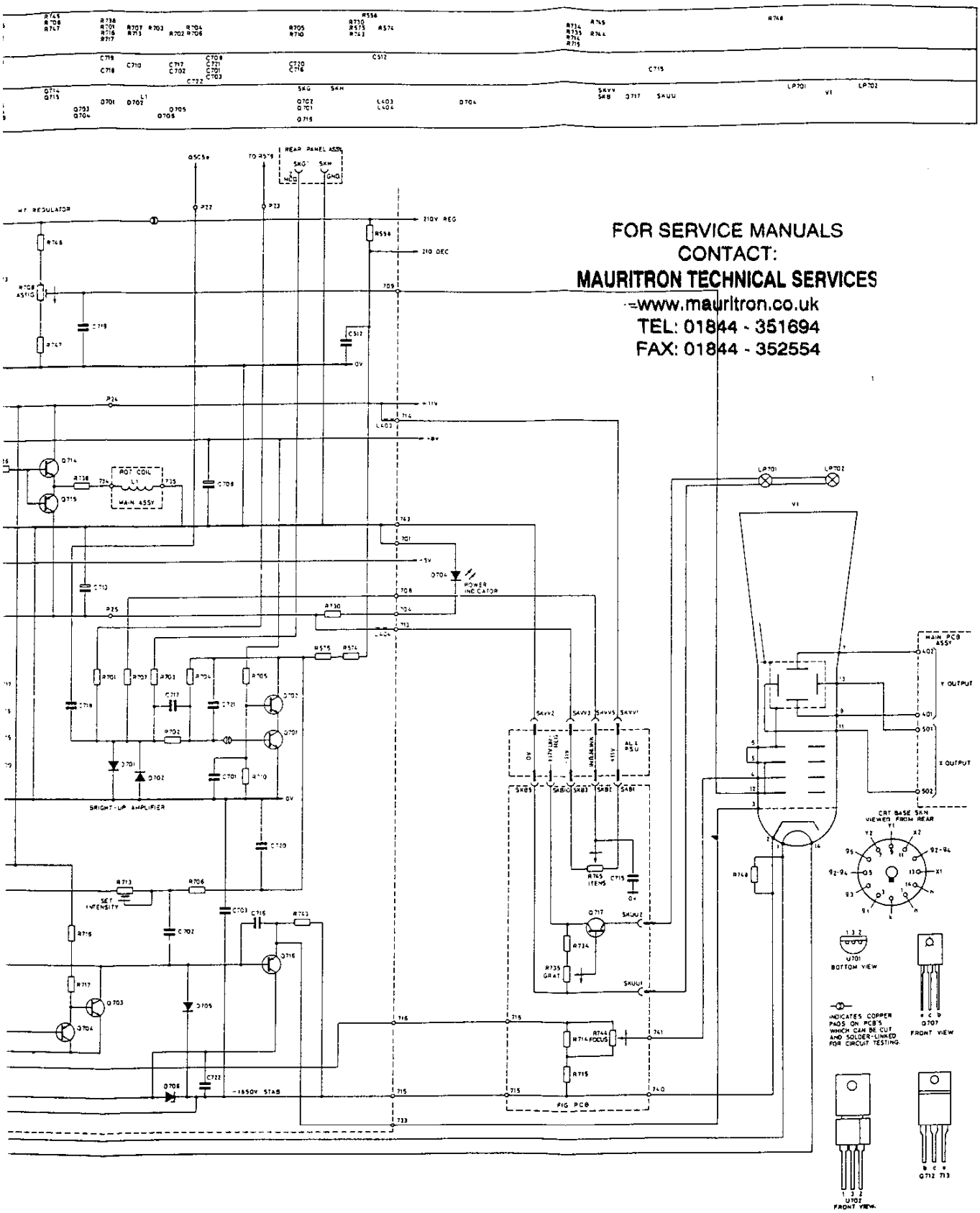
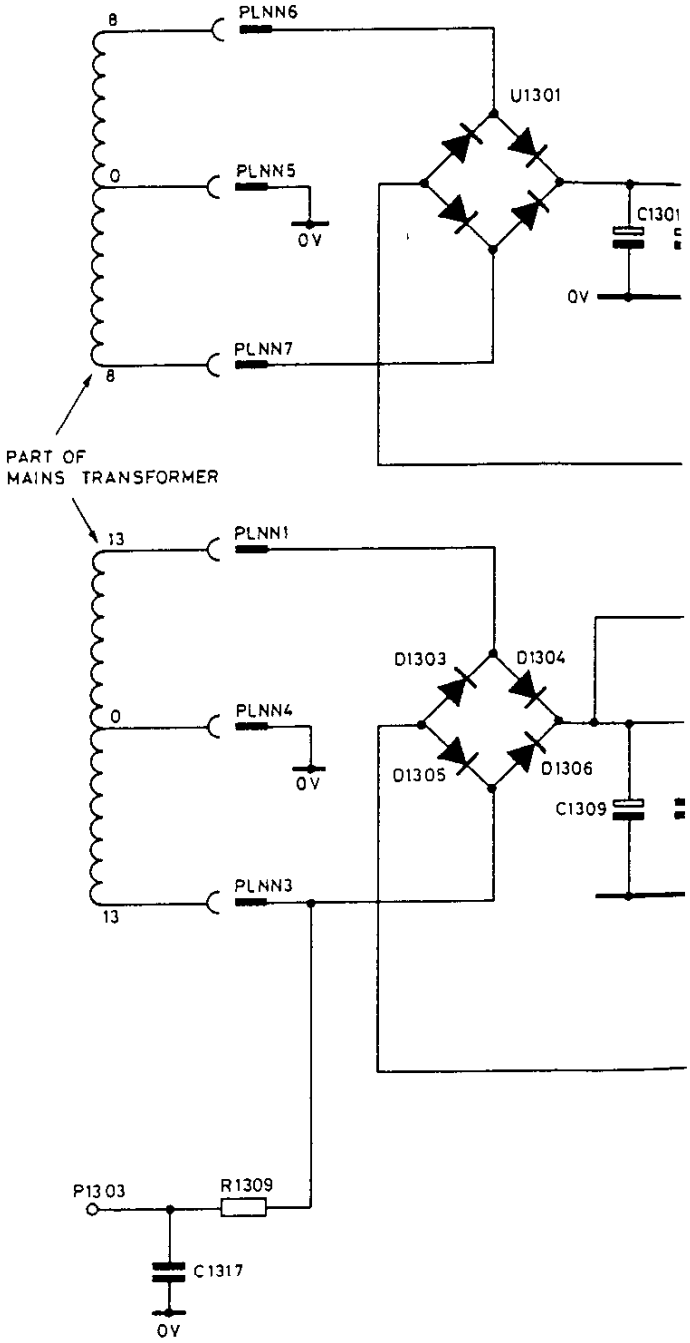


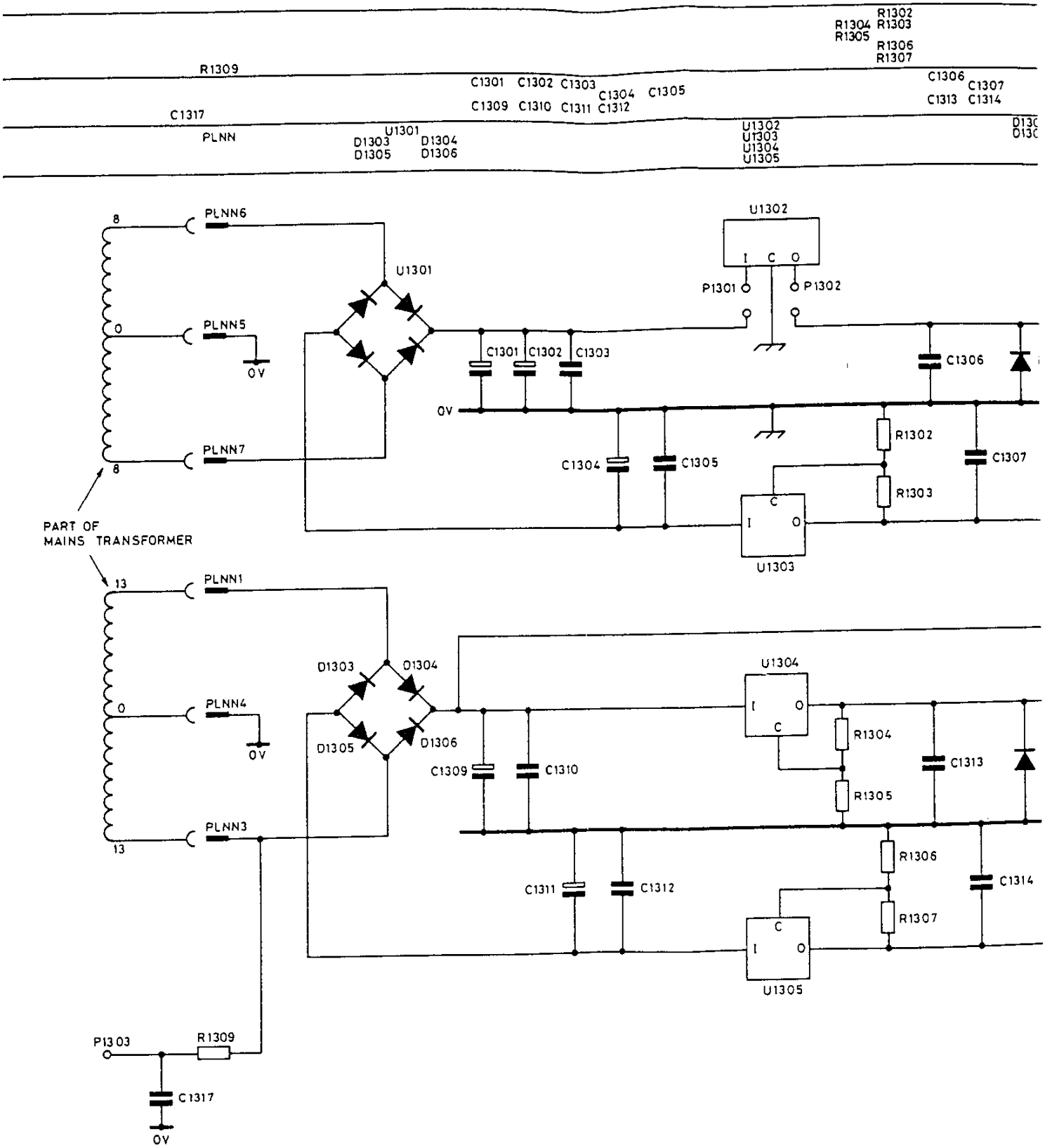
Fig. 28. Power Supply & CRT (Analogue) Circuit Diagram

ction 6

RES.	R1309
CAPS.	C1317 C1301 C1309
MISC.	PLNN U1301 D1303 D1304 D1305 D1306

ating	Part No
0V	43498
5V	34895
5V	34895
0V	43498
	51382
	51382
	23462
	23462
	23462
	23462
	51382
	51382
00V	451943
	47059
	44842
	40731
	44842




R1309
C1317
PLNN
U1301
D1303
D1304
D1305
D1306
C1301
C1302
C1303
C1304
C1305
C1309
C1310
C1311
C1312
U1302
U1303
U1304
U1305
R1302
R1303
R1304
R1305
R1306
R1307
C1306
C1307
C1313
C1314
PLNN6
PLNN5
PLNN7
PLNN1
PLNN4
PLNN3
0V
P1301
P1302
PART OF
MAINS TRANSFORMER
P1303

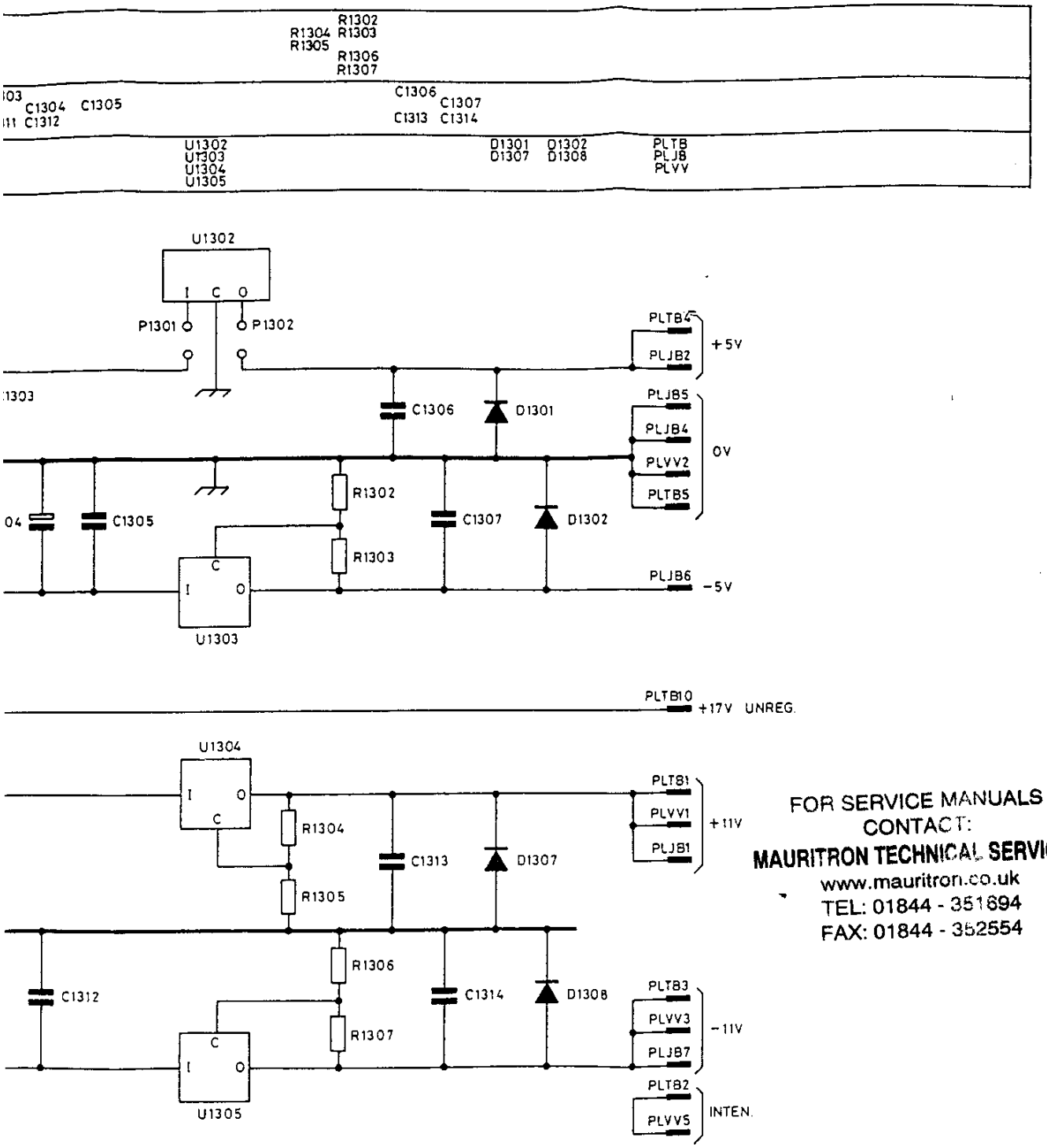


Fig. 29. Power Supply Circuit Diagram

1094/U

nector
(IEEE)

nm)

an Hd. Posi.

pe B

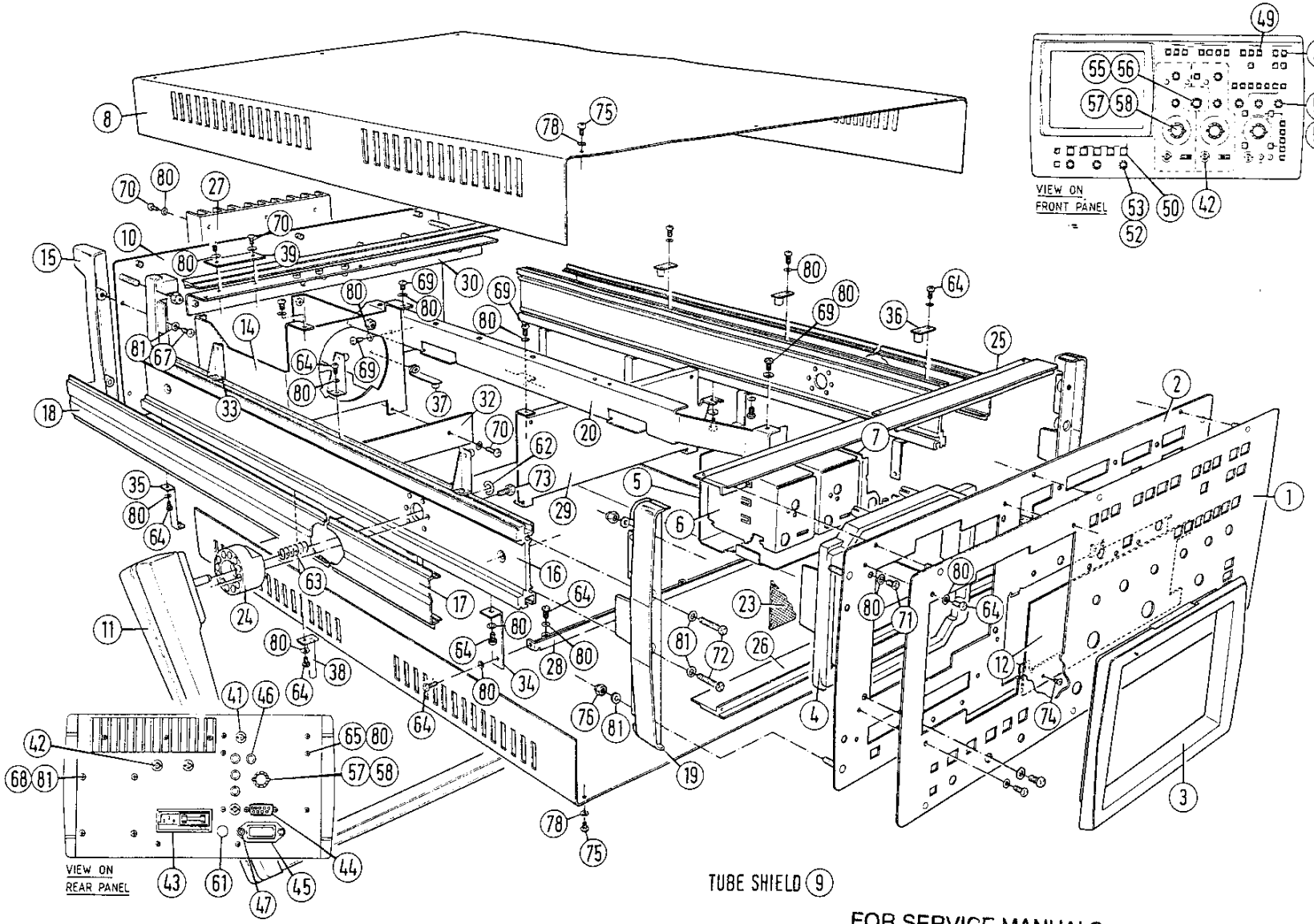


Fig. 30. Mechanical View

4035 MECHANICAL PARTS LIST

Item No.	Part No.	Description
1	452772	Panel Front Composite
2	452888	Panel Front Inner
3	452083	Bezel C.R.T. Moulding
4	44406	Moulding Support C.R.T. (Front)
5	453125	Screen (Plug in Unit)
6	453617	Screen Attenuator
7	453616	Screen Timebase
8	453395	Cover (Top & Bottom)
9	452276	Tube Shield
10	452879	Rear Panel
11	452233	Handle Assy.
12	453615	Front Panel Inner (Small)
13		
14	453365	Bracket C.R.T. Support
15	452284	Foot – Rear Support Moulding
16	452299	Side Support Bar
17	453132	Side Trim – Front
18	453133	Side Trim – Rear
19	453136	Corner Frame Die Cast
20	450648	Heatsink
21		
22		
23	453769	Filter Grey
24	453353	Block Indexing Handle
25	453135	Frame Extrusion (Front – Top)
26	453134	Frame Extrusion
27	453373	Heatsink (Rear Panel)
28	452314	Hinge (Support Bar)
29	453446	Screen (Fast Ram P.C.B.)
30	453374	Heatsink Power Supply
31		
32	452296	Screen Display Pots.
33	453368	Bracket (IEEE Support)
34	452288	Bracket 'L'
35	452289	Bracket 'Z'
36	452286	Support Pillar
37	452290	Bracket
38	452287	Support Pillar
39	452254	Plate Clamping
40		
41	26587	Connector 50Ω B.N.C.
42	1222	Connector 50Ω B.N.C. UG1094/U
43	42266	Socket Power Filter
44	452181	15 Way I.D.C. D-Type Connector
45	452361	24 Way Ribbon Connector (IEEE)
46	23636	Socket, 4mm Black
47	450404	Shouldered Stud (IEEE)
48	453236	Bezel-Pushbutton
49	452067	Knob-Pushbutton
50	452567	Knob-Pushbutton
51	452316	Knob (STD 'D' Shaft 4mm)
52	452117	Cap W1-200 10mm
53	452110	Knob R2-230 10mm x 4
54		
55	452317	Knob (Wing 'D' Shaft 6.35mm)
56	452118	Cap W1-300 15mm
57	452115	Knob R4-450-02 21mm x ¼
58	452126	Cap W1-400 21mm
59		
60		
61	452431	Hole Plug Black (2643)
62	32626	Circlip
63	42645	Spring Compression
64	33037	Screw M3 x 6 Pan Hd. Posi.
65	33039	Screw Mx x 10 Pan Hd. Posi.
66		
67	33048	Screw M4 x 20 Pan Hd. Posi.
68	33046	Screw M4 x 12 Pan Hd. Posi.
69	33069	Screw M3 x 8 Pan Hd. Posi.
70	33041	Screw M3 x 16 Pan Hd. Posi.
71	44579	Screw No. 6 x 3/8 Type B Pan Hd. Posi.
72	452524	Screw M4 x 16 Tap. Pan Hd.
73	41764	Screw M4 x 10 Hex. Hd.
74	33069	Screw M3 x 8 C'sk Hd. Posi.
75	450460	Screw No. 4 x 3/8 GKN Type B
76	33028	Nut Hex. M4 Stiff
77		
78	33003	Washer Plain M3
79		
80	33016	Washer Wavey M3
81	33017	Washer Wavey M4
82		